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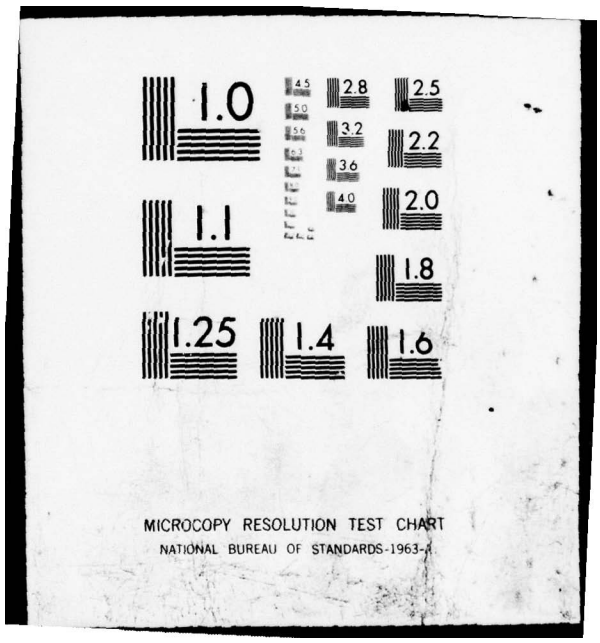
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MARCH 1977

USER MANUAL

EXPLORATORY SYSTEMS CONTROL MODEL (ESM)

for

THE DEFENSE COMMUNICATIONS AGENCY
WASHINGTON, D.C. 20305

Burroughs Corporation
Federal and Special Systems Group
Paoli, Pa. 19301

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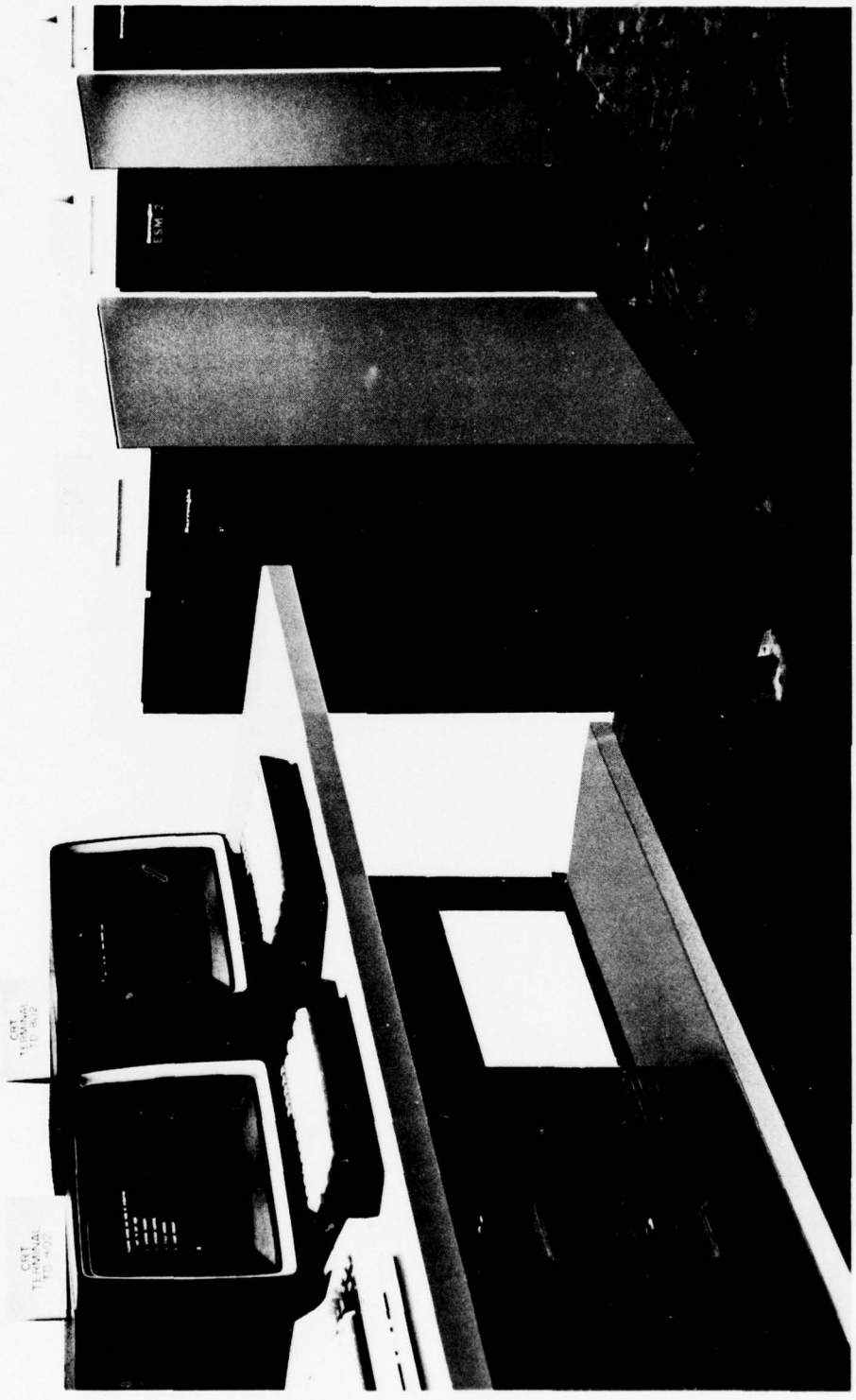
FOREWORD

This publication is the User Manual for the Exploratory Systems Control Model (ESM). It describes the system, each capability and how to use it. This manual was prepared by Burroughs Corporation and is submitted in accordance with the requirements of contract DCA 100-75-C-0054.



Exploratory Systems Control Model (ESM)

SECTION 1

INTRODUCTION

1.1 PURPOSE

The Exploratory Systems Control Model (ESM) provides a flexible tool for simulating and comparing a wide range of system control architectures and their related procedures and protocols. The ESM has been designed to model the class of system control architectures that have the characteristics of decentralized operation, modularity, easy modification and upgrade capability, high reliability, high survivability and fail-soft operation.

1.2 BACKGROUND

The following is based on information in the Statement of Work for contract DCA100-75C-0054.

The control and management of a large communication system is a complex task. It includes the continual monitoring and assessment of system performance, the formulation and implementation of control actions in response to system performance degradation, the detection, isolation and restoral of faults and the generation of analyses, reports and displays in support of the system planning and engineering process. In order to carry out these functions, system controllers require ADP equipments which are geographically distributed and in constant interaction and communication with each other.

In recent years there has been considerable interest in more automated techniques for systems control. The Assistant Secretary of Defense for Telecommunications (now known as DTACCS) stated in guidance for submission of the FY 75-79 program objective memorandum that the DCA effort in the area of automatic system control and technical control should be expanded. The Defense Communications System (DCS) must be a highly survivable entity in order to insure that its vital mission is carried

out. In order to enhance system survivability, it is highly desirable to decentralize the real-time monitoring and control process as much as possible. Therefore, if the system is fragmented the remaining system control elements will be able to effectively operate their fragmented portions of the DCS.

Based on these requirements, the Exploratory Systems Control Model will be used to evaluate and compare candidate system control architectural alternatives. To satisfy these functional requirements, Burroughs has designed and implemented the ESM based on a distributed control concept developed at Burroughs Corporation. The basic concept is a bus, in the form of a ring, in which data flows in one circular direction. Ring interfaces interact with this ring at points called "nodes." A node can pass data through itself along the ring, extract data from the ring, or inject data into the ring. With these functional features, ESM provides an excellent test facility for controlled experimentation with future system control architecturally related functions and concepts.

More specifically the ESM will be used as a tool in the study of such DCS control functions as the following:

1. Evaluation of future DCS control architecture, software, procedures, protocols, etc., to determine how future DCS control could best utilize the Automated Technical Control Program (ATEC), TRI-TAC Communication Control Facilities (TCCF), and other related programs as well as how these programs could be modified, if required, and deployed to support DCA requirements.

2. Provide a flexible tool for determining how the transition from near-term to long-term system control functions can be best accomplished.

1.3 SYSTEM ELEMENTS AND CONNECTIVITY

The ESM is a communications system used to interconnect terminals to host computers so that any terminal can interface with any host for information transfer. To accomplish this, each ring is supplied with devices called "nodes" that act as interfaces from ring to CRT, from ring to host, and from ring to ring. The ring-to-ring nodes are called "gateway" nodes. Each node is the same physically as any other node except for a small amount of special separable hardware for each type of node. The major difference between nodes is in the software of the nodes.

The nodes provide all the necessary communications functions of queueing, parity checking, ACKing, NAKing, retransmitting, alternate routing, etc. The hosts and terminals need only supply the data processing functions and need not be concerned with the communications functions.

The ESM configuration is shown in Table 1-1 and Figure 1-1. The Government-furnished hosts are DEC PDP-11/40 computers. The gateway node interchanges are via cables in the ESM configuration, but in principle can be via any communications medium such as telephone, microwave relay, optical transmission or satellite relay.

The terms "loop" and "ring" are interchangable. Each loop is housed in a separate cabinet in this implementation, but this is not a necessity. A loop could, as easily, extend throughout a building or facility.

Table 1-1. ESM Components (see Figure 1-1)

Ring 1:	2 Gateway Nodes (one to Ring 2 and one to Ring 3)
	1 Host Node to Interface GFE System Control Processor A
	1 GFE Host System Control Processor A (Table 2-3)
Ring 2:	2 Gateway Nodes (one to Ring 1 and one to Ring 3)
	1 Host Node to Interface GFE System Control Processor B
	1 GFE Host System Control Processor B (Table 2-4)
	1 CRT Node to Interface CRT Terminal
	1 CRT Terminal (Table 2-2)
Ring 3:	2 Gateway Nodes (one to Ring 1 and one to Ring 2)
	1 Node to interface future Host processor or terminal
	1 CRT Node to Interface CRT Terminal
	1 CRT Terminal (Table 2-2)

1.4 FEATURES OF THE ESM

The ESM is designed to be transparent to the user. Regardless of the CRT used and the host on which a particular activity takes place, the activity will take place for the CRT that calls for it. When a message is transmitted from a CRT, suitable control bytes are added to the message by the CRT node and directed to the node of a nearby host. When the host receives the message, it will either handle the message completely if it can or it will pass it on to another host, via the ESM, for cooperative handling of the message. This is done under program control using

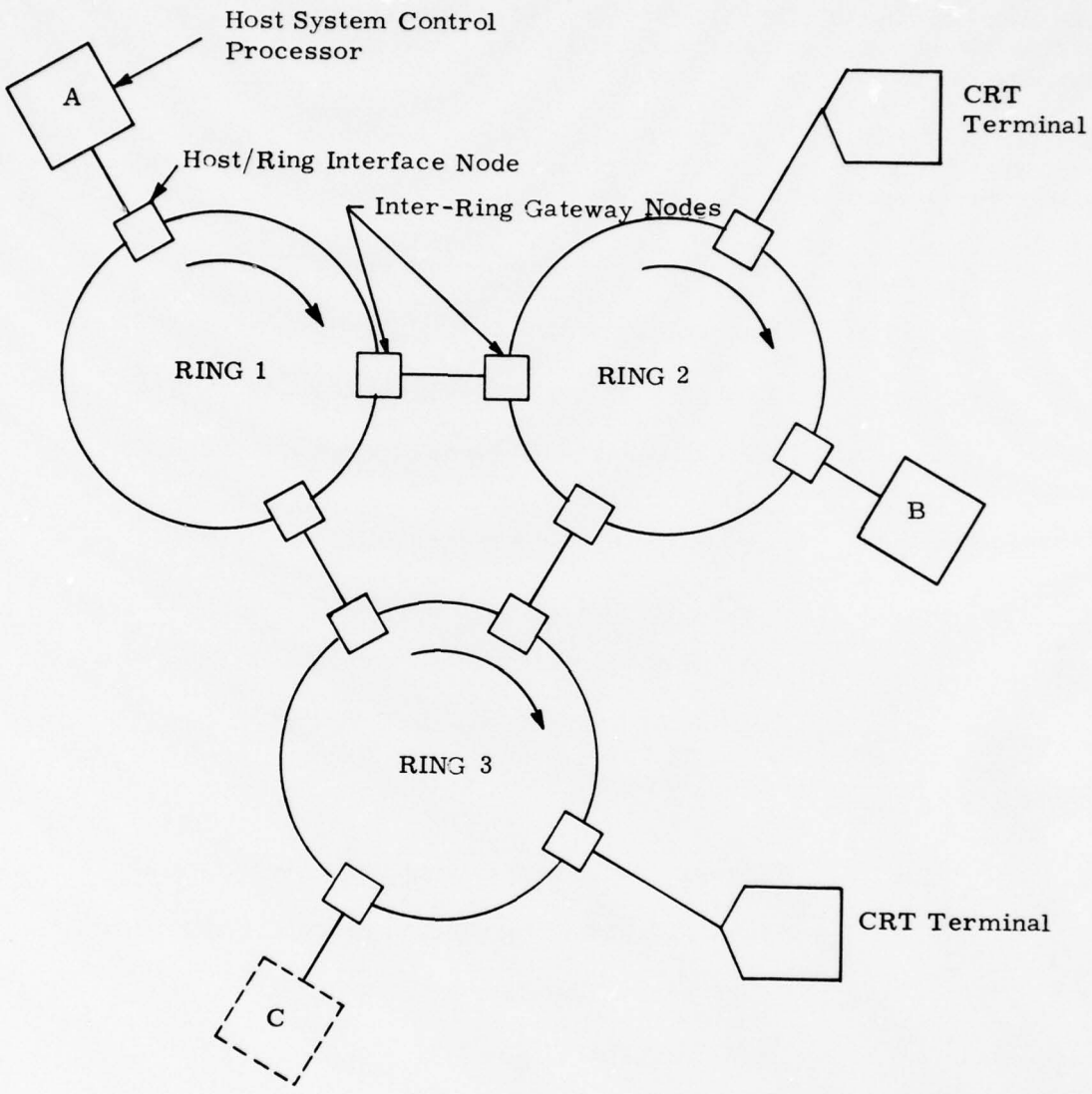


Figure 1-1. ESM Configuration

the content of the CRT message and the added control bytes. The CRT will then receive a response from one of the hosts.

This response will generally be part of the "user language" which is designed to provide directions for further dialog as well as replies to previous messages. The user language description and the method for transmission of messages form a later part of this manual. The language is designed to be modular so that it can be easily updated and enhanced.

Messages are sent in the form of packets of length not greater than 256 bytes. As each packet is sent, the sending node holds it for acknowledgement (ACK) from the receiving node. When an ACK is received by the sending node, it frees the packet space. If a non-acknowledgement (NAK) is received, the message is resent or sent by an alternate route. Absence of an ACK or NAK after a timeout period is considered to be a NAK. After a suitable number of resends without an ACK, the message may be reported "not sent".

Nodes automatically provide input and output queueing for the external device. Sufficient extra memory space is provided in each node to permit receipt of line control protocols from the loop and to act on these protocols. This is done to prevent a deadly embrace condition within the node. If the input queue (from the loop to the external device) is full, new input messages are rejected. Room always exists for the receipt of ACKs and NAKs and other line protocol messages. These are acted upon with dispatch so that they do not reside in data memory for a long period. If the output queue is full, the external device is prevented from sending to the node.

The loop protocols are designed to be non-blocking and self-polling. Each node in the loop has its turn to write onto the loop and if any noise exists on the loop from prior transmissions, it is overwritten by the new transmission. Nodes share the polling activity and any loss of polling is restarted automatically.

ACKs and NAKs are generated by end-user nodes when they receive packets. Each packet is tested against a longitudinal parity byte in the packet. A good check results in an ACK and a bad check results in a NAK.

The user language resides in the hosts. This user language provides dialog and directions to the user so that he can operate the ESM after a very short learning cycle. A file facility exists in the user language which permits the user to access and update file records residing on either host without the need for user knowledge of where they reside. This aspect of the user language permits a distributed file storage capability that is transparent to the user. The user language provides several other modes of operation such as CRT-to-CRT messages and a system inquiry and update capability.

The modeling of a particular system control architecture is a separate programming problem. The user language program may be used to set up the files for the model and to access the files but the architecture modeling program must be added by the user. He may elect either to add the model to the user language or to write a separate program that interfaces to the file modes of the user language.

A specification has been written as a task of the ESM that is aimed toward a more complete implementation of this modeling capability. This specification is given in detail as a separate document. The specification describes a more complete distributed file management capability, a dynamic resource allocation scheme, the details of message transfer in a device-independent fashion using logical identifiers instead of specific terminal addresses, the methods to be used for ensuring that messages are sent to correct destinations, and the methods to be used to ensure continued system operation when simulated system malfunctions occur.

SECTION 2

PHYSICAL CONFIGURATION

The ESM consists of the major physical entities shown on Figure 2-1. These include:

- 3 ESM Loops, each housed in a separate cabinet
- 2 CRT Terminals, Burroughs TD 802's
- 2 Host Processors, PDP-11/40's
- 1 set of interconnecting cables.

These physical entities have a one-to-one relationship to the functional configuration shown in Figures 1-1 and 5-1.

Each of the three loops is contained in a separate cabinet. These cabinets are standard Burroughs B 711-2 completely enclosed cabinets, equipped with backplanes and cooling fans. The backplanes are located in the upper half of the cabinet and provide mounting and interconnecting capability for a total of 90 printed circuit boards arranged in two rows of 45 each. The cabinets are configured to provide for two nodes in the top row and two nodes in the bottom row, with the loop interconnections accomplished on the backplane. Each node consists of 14 pc boards. In addition, two pc boards are required for clock generation and retiming, and two others are required for program loading. Hence, a total of 60 slots are occupied in a completely equipped cabinet (e.g., cabinet #2). Cabinet #1 is equipped with only three nodes. Cabinet #3 is fully equipped, except for a Host Interface Board. In addition, each node is provided with two slots wired to accommodate a plug-in monitor equipped with lights and switches. The monitor provides for manual operation and control of the B 7* microprocessors, and facilitates fault verification and isolation procedures. (See Figure 3-2 for typical ESM cabinet characteristics.)

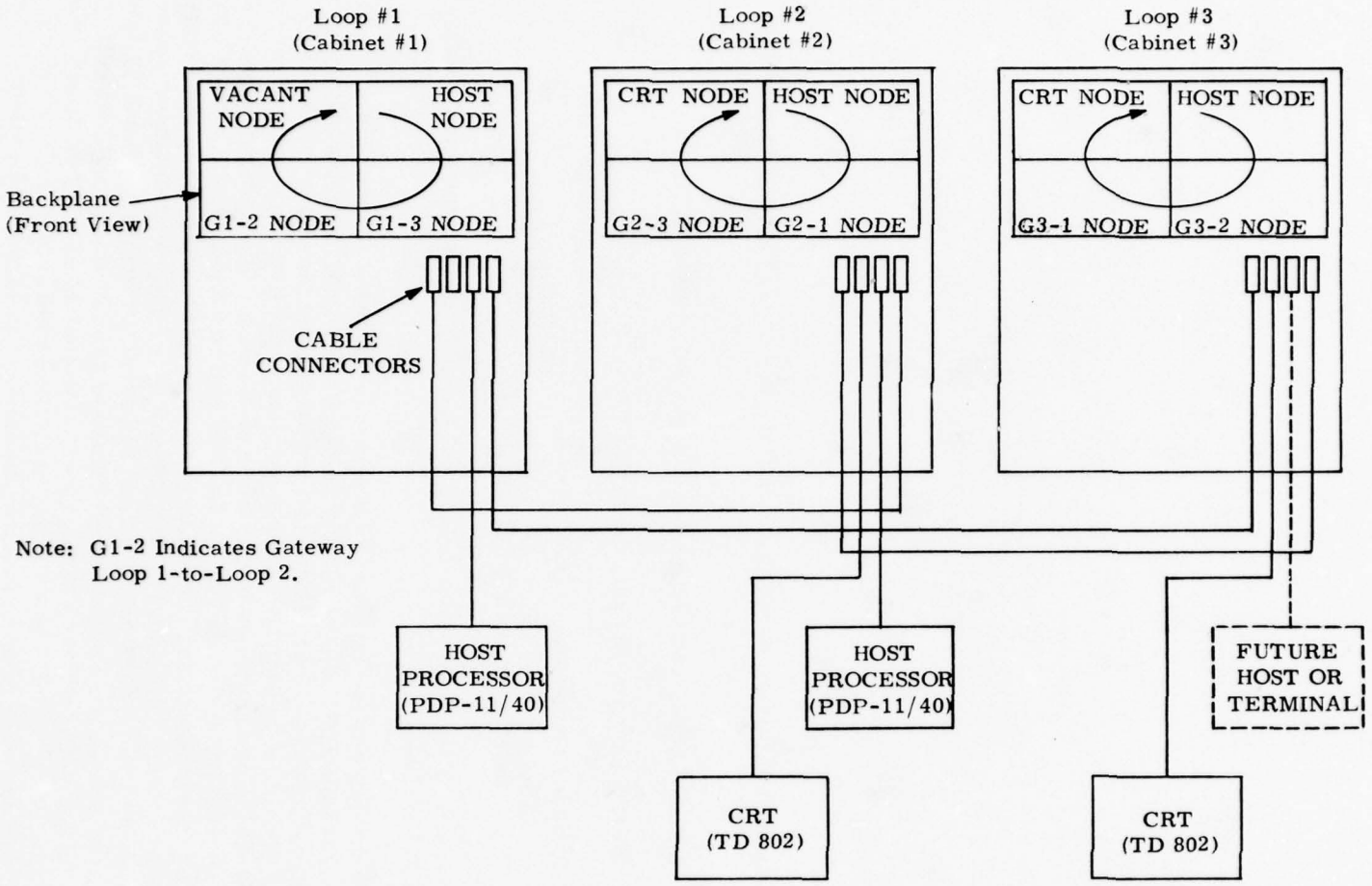


Figure 2-1. ESM Loops (Cabinets)

A power supply is located in the bottom of each cabinet. It has the capacity (75A at 5V) for supporting all logic contained in the cabinet and has adequate margin (4 nodes presently require only 45A) for supporting logic which could be added to the cabinet.

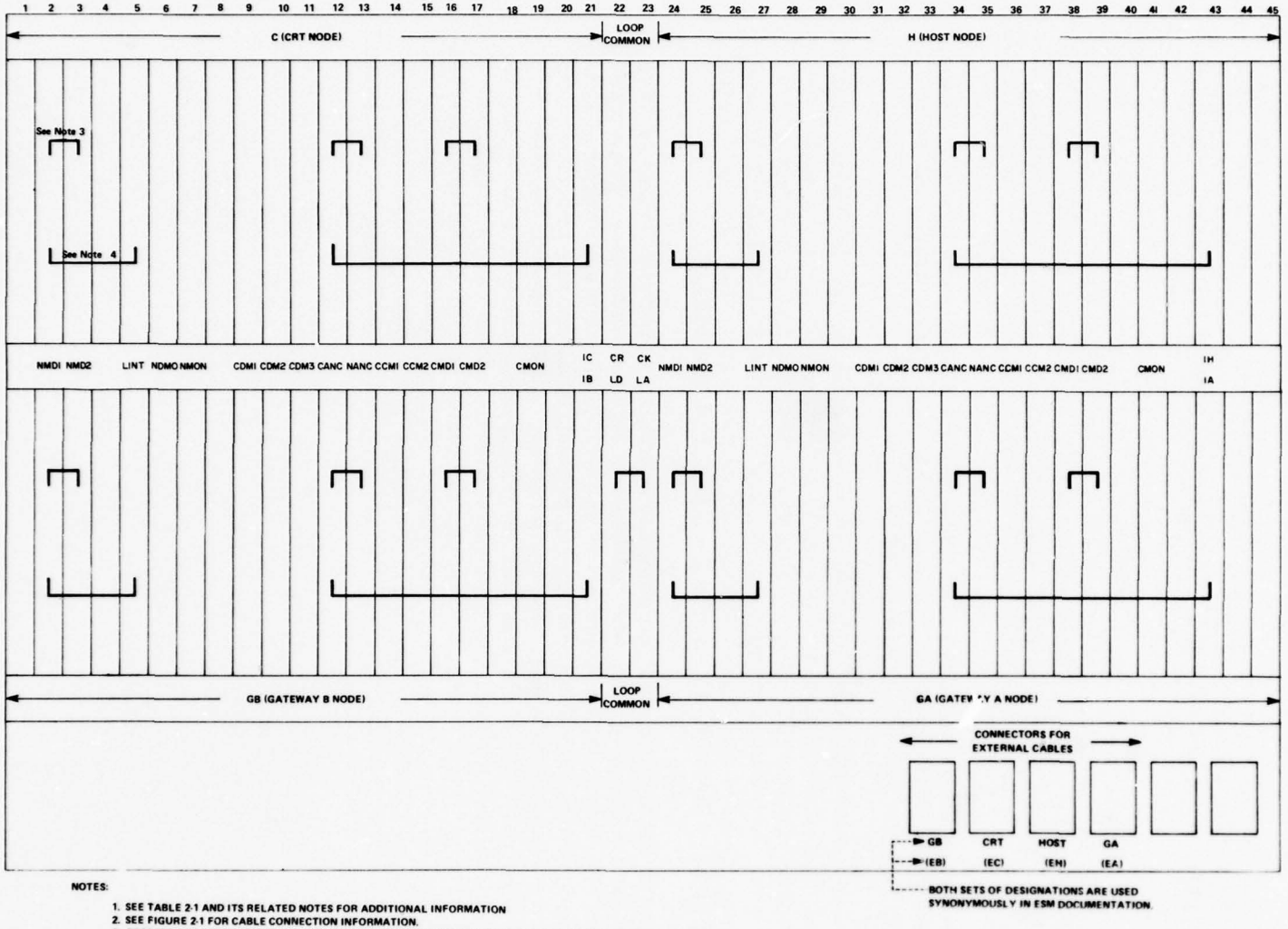
A row of cable connectors is also included as part of the backplane, below the two rows of pc boards. Up to 18 cables could be accommodated, although only 4 are required for ESM interconnections. All backplane connections (both pc boards and cable connectors) are wire wrap type, permitting easy reconfiguration of cabinet wiring.

Figure 2-2 shows the actual location of the pc boards in the card slots of a cabinet. Table 2-1 provides a listing of all of these boards, and cross references pertinent information relating to them.

Operator's controls within the ESM cabinets are of three types: (1) Those mounted on the front edge of the pc boards and used to select the loop speed for each node and the number of nodes in a loop, (2) those mounted on the plug-in monitor and used for manual operation and maintenance, and (3) those mounted on the switch control panel and used for system loading and maintenance. The specific location and use of these controls is detailed in Section 4. 1 of this manual.

As indicated in Figure 2-1, the complete nodes and their interconnecting cabling, which together comprise a loop, are contained in separate cabinets. The arrows on each cabinet, like those on Figures 1-1 and 5-1, indicate the direction of signal flow around the loop. The interconnections between the loops are provided by the cables between pairs of cabinets. Hence, each loop is connected to the other two. Similarly, the Host Processors and CRT terminals are connected to each loop via the indicated cables. All cables are equipped with connectors at each end for easy connection or replacement. Each connector is labeled at each cable end to correspond with its cabinet mounted mating connector. All cables are either flat ribbon or twisted pair and, except for the CRT terminals, enter the cabinets through openings in the bottom of the cabinet. Under-floor routing of cables is anticipated (see Section 3).

The CRT terminals are Burroughs TD 802's, each equipped with keyboard as well as display. These terminals can communicate with the Host Processors, as well as with each other, via the loop interconnections. Each TD 802 can display 24 lines of 80 characters per line. Message preparation is accomplished off-line by typing a message into the terminal's memory while it is simultaneously displayed on the CRT. Editing of the entered message is accomplished prior to transmission. Editing features include complete cursor control, character insert and delete, backspace, tabulate, and forms mode. After completion of editing, the entire message is transmitted in 3-line packet format (up to 256 characters per packet). Positive indication is given to the operator signifying successful transmission. Data is transmitted from, and received by, the TD 802 in an asynchronous mode at a transmission rate of 9600 bits (960 characters) per second. Impending-receipt of a message is signified by an audible alarm if the TD 802 is in the off-line



NOTES:

1. SEE TABLE 2-1 AND ITS RELATED NOTES FOR ADDITIONAL INFORMATION
2. SEE FIGURE 2-1 FOR CABLE CONNECTION INFORMATION.
3. FRONT PLANE CONNECTORS ARE USED TO INTERCONNECT THE FRONT EDGES OF ADJACENT P.C. BOARDS AS INDICATED BY THE SYMBOL ⌐¬.
4. FLAT RIBBON CABLES ARE USED FOR ADDITIONAL INTERCONNECTIONS BETWEEN P.C. BOARDS THAT ARE NOT ADJACENT. THESE INTERCONNECTS ARE SHOWN BY THE SYMBOL └┘.

Figure 2-2. PC Board Locations

(local) state. Further details regarding operation of the TD 802 are provided in Section 4 of this manual and in the Burroughs TD 700/800 Equipment Reference Manual supplied with the TD 802 units. Significant features and options of the specific TD 802 supplied as part of ESM are summarized in Table 2-2

The ESM Host Processors are GFE (Government Furnished Equipment) and are configured as indicated in Tables 2-3 and 2-4. These processors interface with their respective loops via Host Interface nodes per Figures 1-1, 2-1 and 5-1. Data is transferred between the Host Processor and its respective node in bit serial form at a transmission rate of 560 Kbps. Messages are formatted in 128 word (16 bits each) packets for transmission in either direction. Actual interface between the PDP-11/40 UNIBUS and the 560 KHz serial line is achieved via a DEC M1710 Universal Interface Module. This ESM-supplied module was added to each of the two GFE Host Processors.

Table 2-1. PC Board Identification

Slot No.	Slot Ident.	Card Ident.	Part No.	Description
1				Vacant
2	NMD1	MD1	2600-5538M	Part of NCU B7*
3	NMD2	MD2	2600-5561M	Part of NCU B7*
4				Vacant
5	LINT	LIU	LIU	Line Interface Unit
6	NDMO	MPB	2601-8929M2	NCU Data Memory (1K)
7	NMON	(See Note 10)		NCU Monitor Access
8				Vacant
9	CDM1	MPB	2601-8929	CIE Data Memory (1st 4K)
10	CDM2	MPB	2601-8929	CIE Data Memory (2nd 4K)
11	CDM3	MPB	2601-8929M1	CIE Data Memory (Last 3K)
12	CANC	CIE ANC	CIE ANC	CIE Ancillary Logic
13	NANC	NCU ANC	NCU ANC	NCU Ancillary Logic
14	CCM1	7PM	2601-1668M	CIE Control Memory (1st 2K)
15	CCM2	7PM	2601-1668M	CIE Control Memory (2nd 2K)
16	CMD1	MD1	2600-5538	Part of CIE B7*
17	CMD2	MD2	2600-5561M	Part of CIE B7*
18				Vacant
19	CMON	(See Note 10)		CIE Monitor Access
20				Vacant
21 Top	IC	CRT INTF	CRT INTF	Interface Logic, CRT
21 Bott	IB	G'WAY INTF	G'WAY INTF	Interface Logic, Gateway B
22 Top	CR	CR	CR	Loop Clock Retimer
22 Bott	LD	LDR	LDR	Loop Loader
23 Top	CK	CK GEN	CK GEN	Loop Clock Generator
23 Bott	LA	LDR ANC	LDR ANC	Loop Loader Ancillary
24	NMD1	MD1	2600-5538M	Part of NCU B7*
25	NMD2	MD2	2600-5561M	Part of NCU B7*
26				Vacant

B7* is the designation of the Burroughs Microprocessor used in the ESM described herein.

Table 2-1. (Cont.)

Slot No.	Slot Ident.	Card Ident.	Part No.	Description
27	LINT	LIU	LIU	Line Interface Unit
28	NDMO	MPB	2601-8929M2	NCU Data Memory (1K)
29	NMON	(See Note 10)		NCU Monitor Access
30				Vacant
31	CDM1	MPB	2601-8929	CIE Data Memory (1st 4K)
32	CDM2	MPB	2601-8929	CIE Data Memory (2nd 4K)
33	CDM3	MPB	2601-8929M1	CIE Data Memory (Last 3K)
34	CANC	CIE ANC	CIE ANC	CIE Ancillary Logic
35	NANC	NCU ANC	NCU ANC	NCU Ancillary Logic
36	CCM1	7PM	2601-1668M	CIE Control Memory (1st 2K)
37	CCM2	7PM	2601-1668M	CIE Control Memory (2nd 2K)
38	CMD1	MD1	2600-5538	Part of CIE B7*
39	CMD2	MD2	2600-5561M	Part of CIE B7*
40				Vacant
41	CMON	(See Note 10)		CIE Monitor Access
42				Vacant
43 Top	IH	HOST INTF	HOST INTF	Interface Logic, Host
43 Bott	IA	G'WAY INTF	G'WAY INTF	Interface Logic, Gateway A
44				Vacant
45				Vacant

Notes:

1. Slots 1 through 21 in the top row comprise the CRT Node, except for Cabinet #1 (Loop #1) in which these slots are entirely vacant.

2. Slots 22 and 23, in both rows, house boards common to the entire loop.

3. Slots 24 through 45 in the top row comprise the Host Node.

4. Slots 1 through 21 in the bottom row comprise the Gateway B Node.

Table 2-1. (Cont.)

5. Slots 24 through 45 in the bottom row comprise the Gateway A Node.

6. Slot 43 of the top row in cabinet #3 (Loop #3) will be equipped with a Host or terminal interface board in the future, but is presently vacant.

7. Boards in slots 5, 22 top, 23 top and 27 are equipped with RATE SELECTION switches. The Board in slot 22 top is also equipped with an ODD/EVEN switch. See Section 4.1.2.

8. Gateway A (GA) and Gateway B (GB) are in certain instances referred to more specifically as follows:

	Loop #1	Loop #2	Loop #3
GA	G1-3	G2-1	G3-2
GB	G1-2	G2-3	G3-1

Note that G1-3 indicates Gateway from Loop #1 to Loop #3.

9. Only PC Boards having identical part numbers are interchangeable. The letter M after a part number indicates a modification to the basic part number.

10. The ESM monitor described in Section 4.1.4 is plugged into any monitor access slot (slots 7, 19, 29, and 41 of either row) as desired. The monitor is normally removed from the system during regular system operation. Part No. and card Identification for the ESM Monitor are "MON".

Table 2-2. TD 802 Characteristics

1920 Character Display – 24 lines @ 80 characters/line
Character Format – 5 X 7 Dot Matrix
Domestic ASCII Character Set

Data Comm Alphanumeric Keyboard

Point-to-Point Line Discipline

Asynchronous Data Transmission @ 9600 Bps
10-Bit Characters with Even Parity (LSB transmitted first)
On-Line and Off-Line (Local) Capability

Audible Alarm on Incoming Messages (in Local Mode)

Line Activity Indicator

Brightness Control

Audible Alarm Volume Control

Edit Package; including Forms, Tabulate, Character Insert/ Delete, cursor control and backspace.

Dimensions: 15" H X 16 1/2" W X 26" D

Weight: 75 pounds

Power: 120V, 60 Hz, 3A.

Note: For detailed characteristics, see Burroughs TD 700/800 Equipment Reference Manual

Table 2-3. Loop 1 Host Processor Configuration

HARDWARE

Qty.	Model	Description
1	PDP 11/40-BK	PDP-11/40 CPU with 16K word parity core memory, LA36 DECwriter and control (DL11-A), and cabinet.
1	H960-DA	Expansion Cabinet
2	MF11-UP	16K word parity core memory and control with expansion capability to 32K (by addition of MM11-UP), 980 nsec cycle time.
3	MM11-UP	16K word parity expander core memory. Mounts in MF11-UP. 980 nsec cycle time.
1	KW11-L	Line frequency real-time clock. Divides time into intervals of 16 2/3 msec (20 msec @ 50 Hz line frequency). Mounts in a dedicated CPU slot.
1	KW11-P	Programmable real-time clock, program selectable inputs of 100 kHz, 10 kHz, line frequency, or external signal.
1	KT11-D	Memory Management Option. Permits access to 124K words of memory and provides protection and relocation. Includes KJ11-A Programmable Stack Limit Option, which permits a soft stack limit violation.
1	KE11-E	Extended Instruction Set Option. Provides extended manipulation of fixed point numbers, signed integer multiply and divide, and long shifts.
1	MR11-DB	Bootstrap loader for mass storage devices (disks, DECtape, magtape).
2	DB11-A	UNIBUS repeater. Allows an additional 18 unit loads and an additional 50 feet of UNIBUS to be added.
2	DB11-B	Controller Mounting Panel

Table 2-3. (Cont.)

Qty	Model	Description
1	KE11-F	Floating Point Option. Enables faster calculation; floating point add, subtract, multiply and divide.
1	RP11-CE	20 million word disk pack drive and control unit. Expandable to a total of 8 RP03 disk pack drives. 7.5 microsecond/word transfer rate, 42 msec average access time.
1	TMA11-EA	45 inch/sec magnetic tape transport and control unit. Expandable to a total of 8 TU10 transports. 9-track, 800 bpi (industry compatible).
1	VT50-AA	DECscope video terminal. 75 to 9600 baud, switch selectable. 20 mA interface. (Used at 9600 baud in host control processor A.)
1	DL11-C	Current Loop (20 mA) Serial Line interface with customer specifiable speed, character size, parity and stop bit size. (Interfaces VT50-AA to UNIBUS.)
		SOFTWARE
1	QJ625-AD	RSX11-M (Version 2) real-time, disk-based operating system providing event-driven multi-programming and foreground/background capability. Includes: Executive, MACRO assembler, task builder (linker and overlay builder), editor, on-line debugger, librarian, PIP file utility program; file verification, dump, and exchange programs; ANSI Standard FORTRAN IV compiler and run-time system. (Storage medium: 9 track tape).

Note 1: When loaded with the RSX-11D operating system, host control processor A also interfaces a Vector General interactive graphics system, a PDP-11/10 processor connected to an IBM 370/155 computer, and several Preston A/D and D/A converters. These features will not be used in connection with the ESM contract.

Note 2: Of the two clocks (KW11-L and KW11-P) physically installed on host control processor A, only one (and not both simultaneously) can be included in the operating configuration at SYSGEN time.

Table 2-4. Loop 2 Host Processor Configuration

HARDWARE

Qty.	Model	Description
1	PDP-11/40-BS	CPU with 32K word parity core memory, LA36 DECwriter and control (DL11-A).
1	KW11-P	Programmable real-time clock. Program selectable inputs of 100 KHz, 10 KHz, line frequency, or external signal.
1	KT11-D	Memory management option. Permits access to 124K words of memory and provides protection and relocation. Includes KJ11-A programmable stack limit option, which permits a soft stack limit violation.
1	KE11-E	Extended instruction set option. Provides extended manipulation of fixed point numbers, signed integer multiply and divide, and long shifts.
1	BM873-YB	Restart loader contains ROM with bootstrap program for paper tape, disk, magnetic tape, DEC tape, and DEC cassette.
1	DD11-B	Peripheral mounting panel. Includes UNIBUS connector module M920. Accommodates up to 4 small peripheral controllers or 2 DF11's with DL11's and 2 small peripheral controllers.
1	KE11-F	Floating point option. Enables faster calculation; floating point add, subtract, multiply, and divide.
1	RK11J-DE	1.2 million word disk cartridge drive and control unit. Expandable to a total of 8 RK05 DEC-pack disk drives. Eleven microsecond/word transfer rate, 70 msec average access time. Included cabinet has space for 3 additional RK05's.
2	RK05K-11	Cartridge for RK05 (1.2 million words).
1	TMA11-EA	45 inch/sec magnetic tape transport end control unit. Expandable to a total of 8 TU10 transports. Nine track, 800 bpi (industry compatible).

Table 2-4. (Cont.)

Qty.	Model	Description
1	VT52-AA	DECscope video terminal. 75 to 9600 baud, switch selectable. (To be used at 9600 baud.) 123 ASCII character keyboard, 96 characters displayable (7×7 character matrix). 20 mA current loop interface.
1	DL11-A	Current loop (20mA) serial line interface to VT52 at 9600 baud. Eight bit character size; 2 stop bits.
		SOFTWARE
1	QJ620-AD	RSX11-M (Version 2) real-time disk-based operating system providing event-driven multiprogramming and foreground/background capability. Includes: Executive, MACRO assembler, task builder (linker and overlay builder), editor, on-line debugger, librarian, PIP file utility program; file verification, dump, and exchange programs; ANSI standard FORTRAN IV compiler and runtime system. (Storage medium; 9 track tape.)

SECTION 3

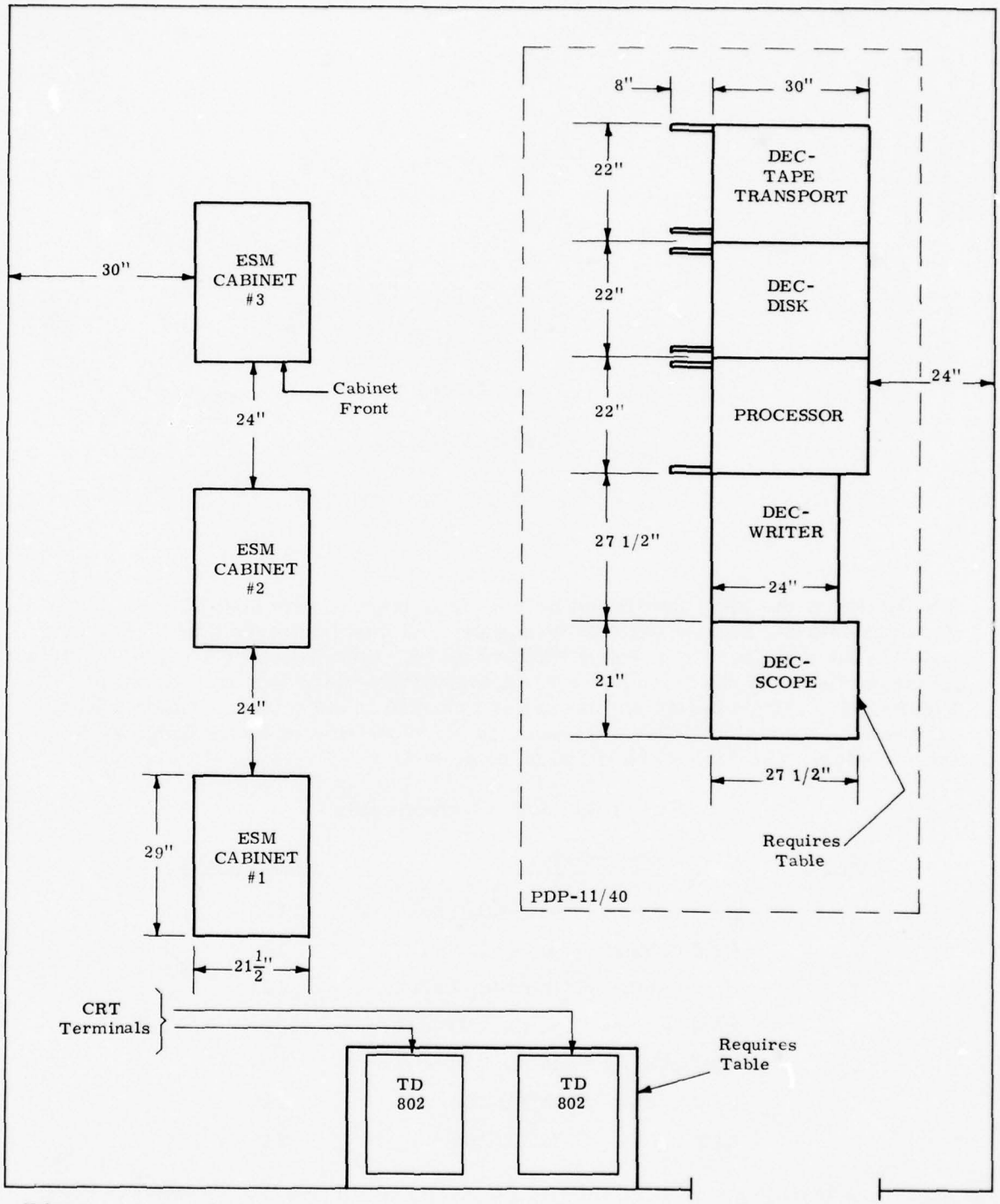
INSTALLATION

Installation of the ESM, as defined herein, is concerned with installing the three ESM cabinets and the two TD 802 Terminals, and interfacing them with each other and with the two Host Processors (PDP-11/40's). Installation of the PDP-11/40's is accomplished by the manufacturer. A typical floor plan layout is shown in Figure 3-1. Figure 2-1 shows the cables provided to interconnect major system elements. Separation of these elements is therefore limited by the lengths of these cables. The cables are listed in Table 3-1.

Table 3-1. System Cables

Qty.	Description	Length (ft.)
1	ESM cabinet #1 to cabinet #2	12
1	ESM cabinet #2 to cabinet #3	12
1	ESM cabinet #1 to cabinet #3	18
1	ESM cabinet #1 to Host Processor	100
1	ESM cabinet #2 to Host Processor	25
1	ESM cabinet #2 to TD 802	24
1	ESM cabinet #3 to TD 802	24

All cables are equipped with connectors at each end. These connectors are compatible with mating connectors provided on the equipment. Also, the connectors on the cables as well as the mating connectors on the equipment are identified with appropriate labels to insure correct connection.



Notes
1. Only the Host Processor connected to ESM Loop 2 (Cabinet #2) is shown.
2. All dimensions shown are approximate.

Figure 3-1. Typical System Floor Plan

Figure 3-2 shows the physical characteristics of the ESM cabinets. The cabinets are mounted on casters, but are expected to remain relatively stationary. The cabinets should be oriented as shown on the floor plan (Figure 3-1) for ease of operation and maintenance. Start-up and restart procedures require opening the front door which requires a minimum of 24 inches between cabinets (see Figure 3-1). Maintenance and installation procedures require removing the lift-off side panels. Note that the panel retaining bolts at the bottom of the cabinet must first be loosened. Maintenance access clearance of at least three feet should be provided on each side of the cabinet.

All cables, including a-c power cord, exit the cabinet via a cable opening in the bottom of the cabinet (Figure 3-2). All cabling is to be routed under the false floor. Also, a-c power connections are to be under the false floor. A-c power connection is via standard 3-wire, 6-foot power cord equipped with plug. Power required is 105-125V, 60 Hz, as follows:

ESM cabinet #1	5A
ESM cabinet #2	7A
ESM cabinet #3	7A

Configure power supply strapping for actual input voltage per information on rear plate of power supply.

A view of an ESM cabinet with side panels removed is shown in Figure 3-3.

The TD 802 Input and Display terminals are to be located on a table(s). Overall dimensions are per Figure 3-4. Installation is limited to plugging-in the a-c power cord and the appropriate signal cable (Figure 2-1). A-c power required is 120V, 60 Hz at approximately 3A. Connection is via standard 3-wire, 6-foot a-c power cord. A convenient wall mounted a-c outlet should be available. The signal cable connects at the rear of the terminal and is to be routed under the false floor to the appropriate ESM cabinet.

Connection of the cables from the ESM cabinet at the PDP-11/40's must be made directly to the PDP-11/40 interface board provided with the ESM. This board, the M1710 Universal Interface Board, must first be installed in an SPC slot of each PDP-11/40 Processor. The cable is then routed through the bottom of the PDP-11/40 cabinet and plugged into the connector already mounted on the M1710 Board.

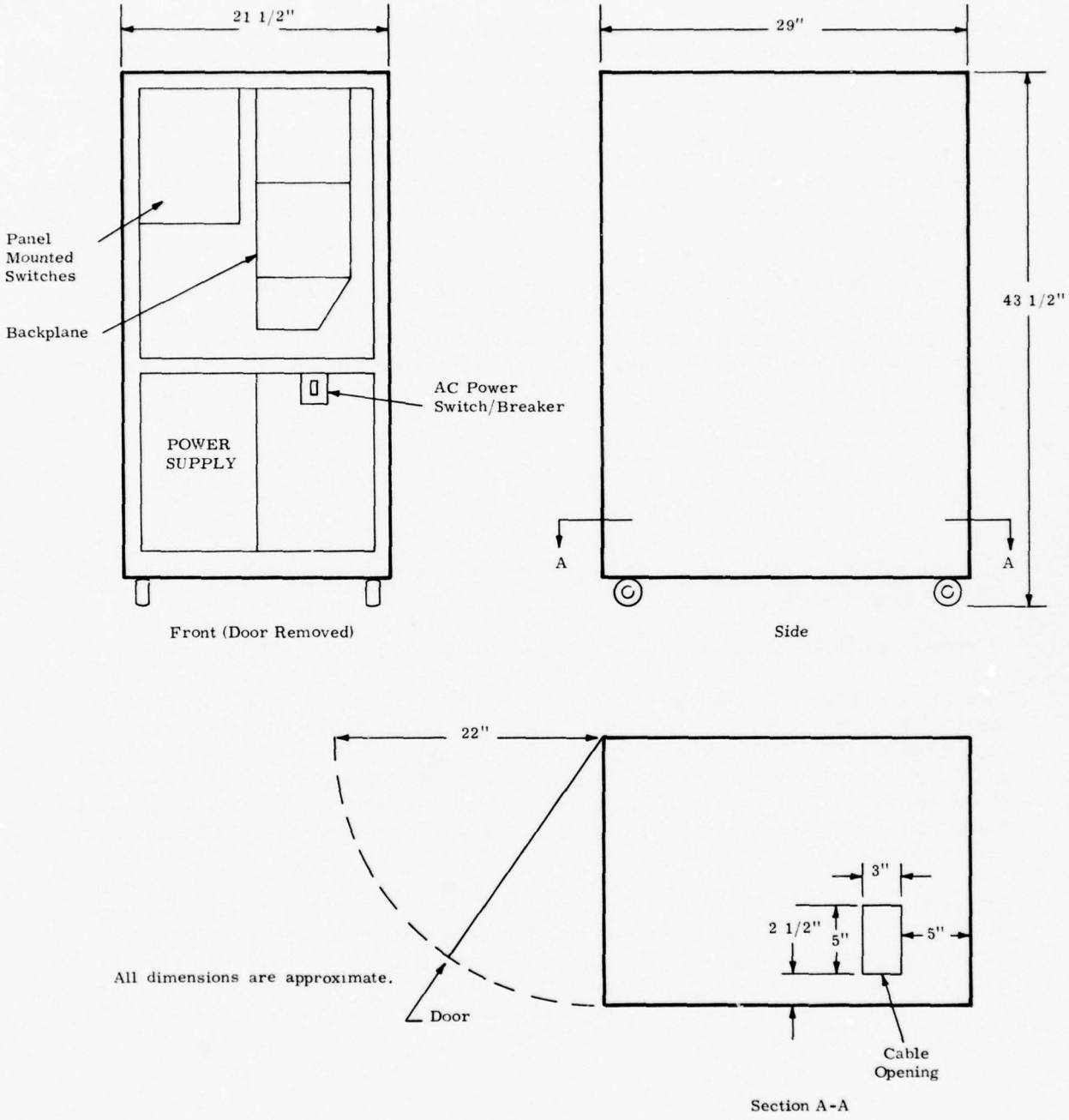


Figure 3-2. ESM Cabinet - Physical Characteristics

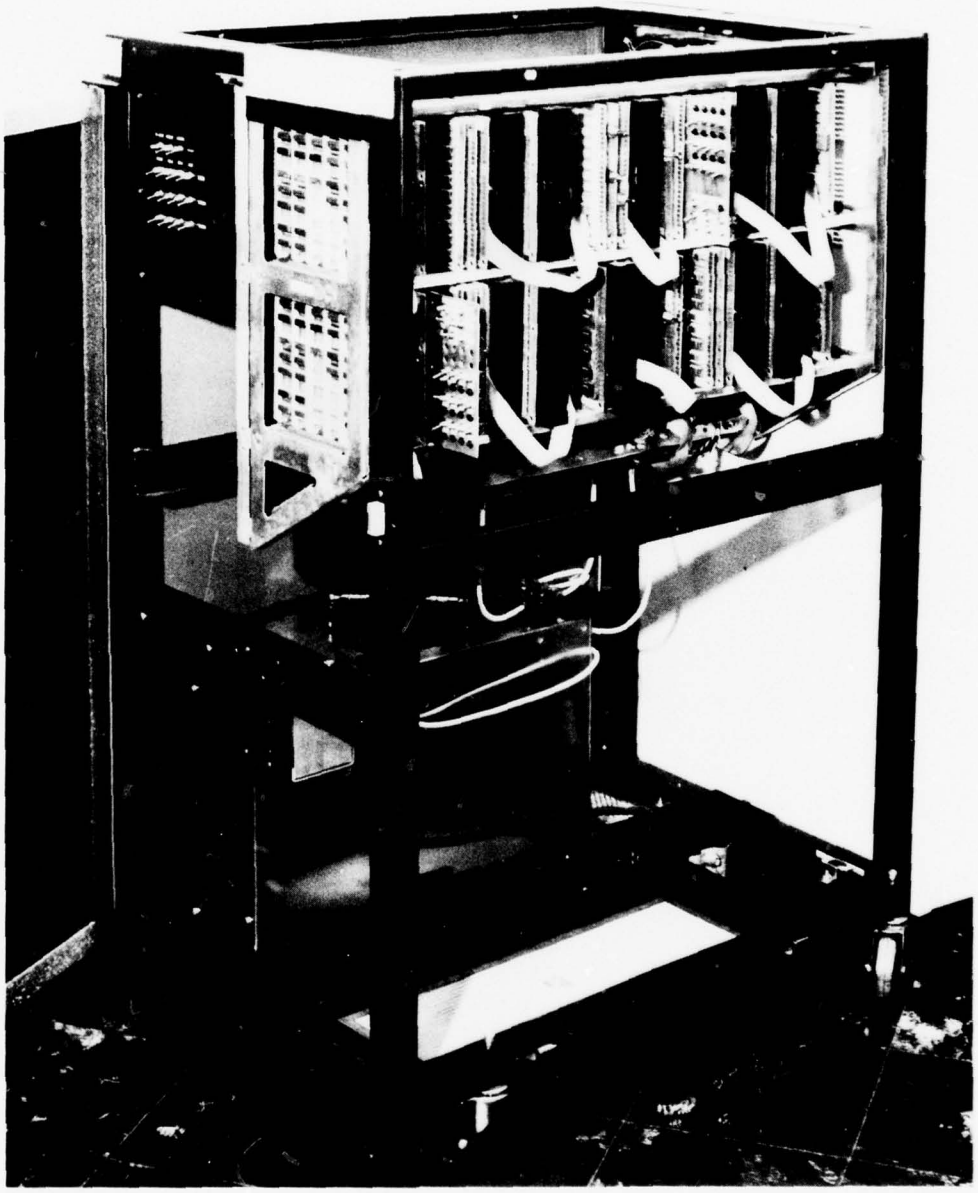
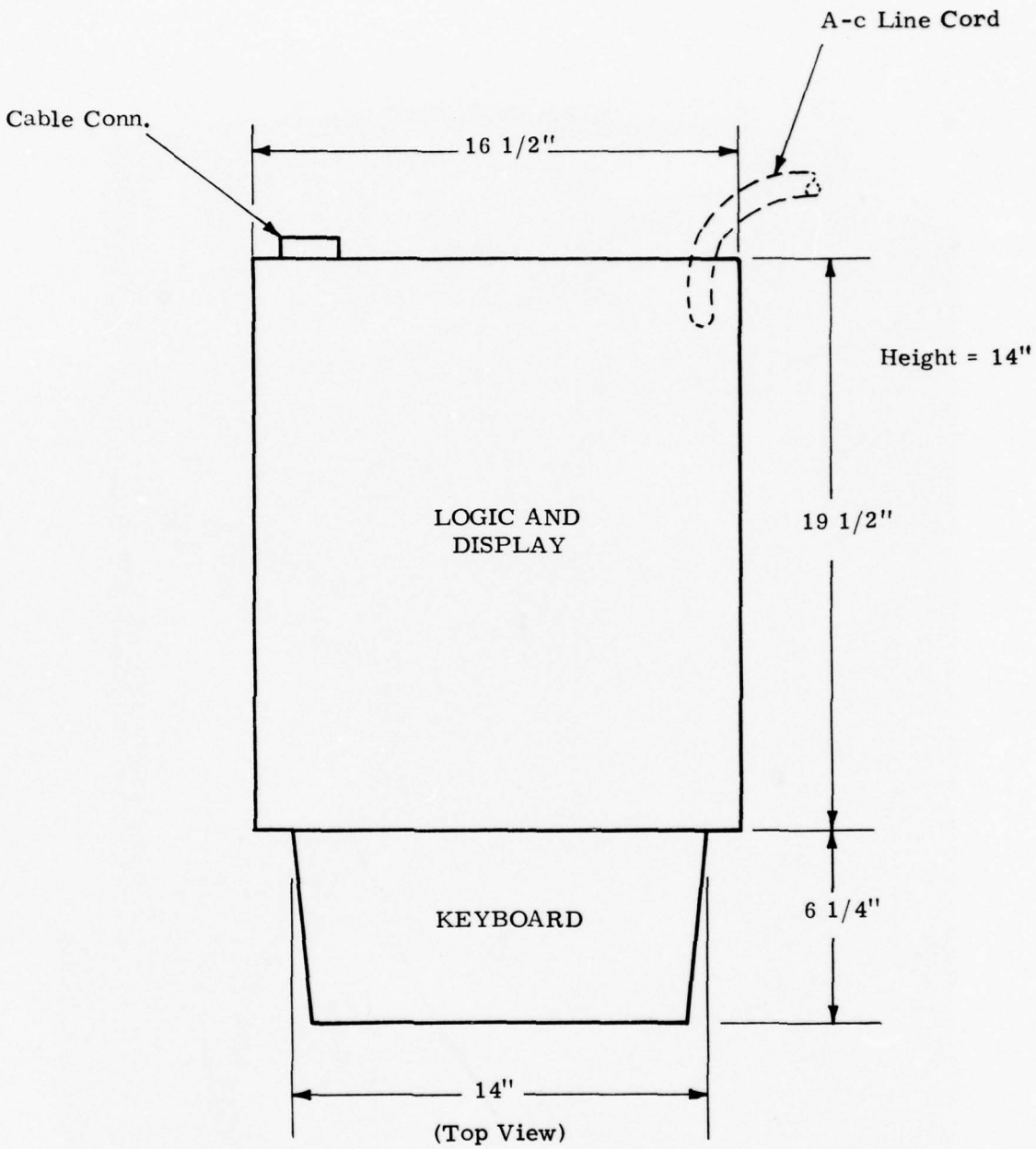


Figure 3-3. ESM Cabinet, Side Panels Removed



All dimensions are approximate.

Figure 3-4. TD802 - Physical Characteristics

SECTION 4

OPERATING CONTROLS AND PROCEDURES

This section provides the information required for operation of the ESM. It is assumed that the operator is proficient at using the PDP-11/40 processors and their associated peripherals. The operator is also referred to the Burroughs TD 700/800 Equipment Reference Manual for operation of the TD 802's.

The information in the following paragraphs focuses on the operation of the ESM Loop Cabinets and the overall ESM System. This information is provided in the following subsections:

1. Operator's controls
2. System Tapes
3. System Startup
4. User Language
5. Maintenance and Diagnostics
6. Microcode Assembler.

4.1 OPERATOR'S CONTROLS

Operator controls as described herein are those associated with the ESM cabinets of Figure 3-2. They are described here in four categories:

1. Power controls
2. Panel-mounted controls
3. Card-mounted controls
4. ESM monitors.

4.1.1 Power Controls (On-off Switch, Breakers and Fuses)

Each ESM cabinet is equipped with:

1. A combination a-c, on-off switch and circuit breaker (see Figure 3-2), rated at 15A, and used for a-c protection as well as on-off control.

2. A d-c, on-off switch and circuit breaker, located at the top front of the power supply and used for d-c protection of the 75A, 5V output of the power supply.

3. Fuses

   a. Two 30A, 32V, 5AG Fuses. Each fuse distributes 5V power to one half of the backplane. These fuses are mounted at the top rear of the power supply.
   Note: Cabinet 1 uses one 30A fuse and one 15A fuse. The 15A fuse is for the left half (partially equipped) of the backplane.

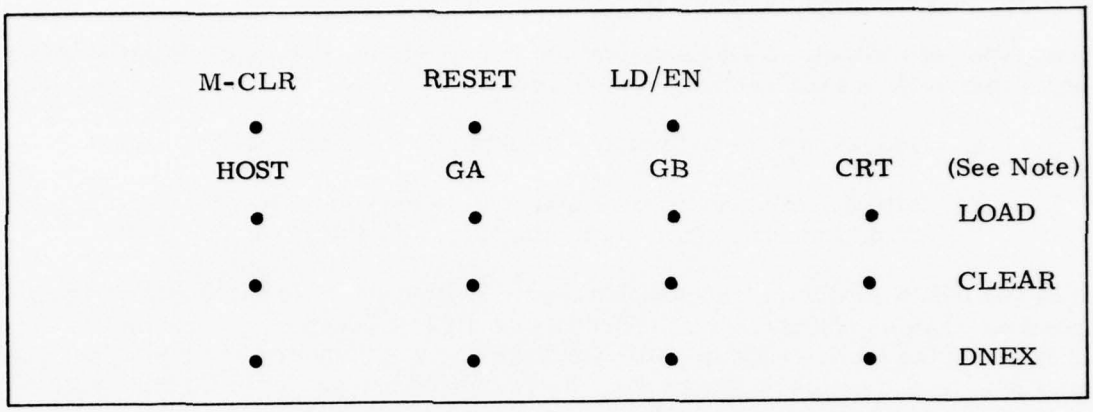
   b. Two 1/2 A, 125V, 3AG Fuses. One is used to protect the a-c input of the cabinet fans; the other is used to protect the a-c input of the power supply fan. These are in-line fuses.

   c. One 2A, 250V, 3AG Fuse. Protects the +12V output (presently unused) of the power supply, mounted at the top front of the power supply.

   d. One 3/4 A., 250V, 3AG Fuse. Protects the -12V output (presently unused) of the power supply, mounted at the top front of the power supply.

4.1.2 Panel Mounted Controls (Switches)

The Panel Mounted Controls are located in the cabinet as shown in Figure 3-2. This Panel is detailed in Figure 4-1. Access to this panel is by opening the cabinet front door. These switches are used for start-up, loading, restarting and maintenance operations. The switches are described in Figure 4-1 and are referred to throughout the paragraphs of this section.



Switch Functions

M-CLR (MASTER CLEAR): Sets all B7*'s in cabinet (both NCU and CIE to MPCR = 0

RESET: Removes non-zero information circulating on the loop. Inserts zeros in all C and D fields.

LD/EN (LOAD/ENABLE): Puts all B7*'s into a "Don't Execute" state. Used in loading with Load switches.

LOAD: Up position for loading.

CLEAR AND DNEX Rows: Used for debugging individual nodes. Clear sets Nodes CIE and NCU to MPCR = 0; DNEX puts Nodes (both NCU and CIE) In "Don't Execute" state.

NOTE: The column headings HOST, GB, GA and CRT refer to those respective nodes within the cabinet. The GB and GA designations are only for reference to the actual designations which vary per cabinet, as follows:

	Cabinet #1	Cabinet #2	Cabinet #3
GA	G1-3	G2-1	G3-2
GB	G1-2	G2-3	G3-1

(See Figure 2-1 for physical location of nodes).

Figure 4-1. ESM Cabinet Control Panel

4.1.3 Card-Mounted Switches

Two types of switches are mounted on the front edge of certain PC Boards (Figure 2-2 and Table 2-1) in each cabinet. These are:

1. Odd/Even Node Selection - Mounted on the Clock Retimer card

2. Rate Selection Switches - Mounted on the Clock Generator card, Clock Retimer card, and each Line Interface Unit Board.

The ODD/EVN switch (a two-position toggle switch) is set to the ODD, or Up, position when an odd number of nodes is installed in a loop (e.g., cabinet #1). It is set to the EVN, or Down, position when an even number of nodes is installed in a loop (e.g., cabinets #2 and #3). Its position should be changed only when a cabinet (or loop) is reconfigured.

The Rate Selection Switches are three-position toggle switches, wherein each position represents one of the three selectable rates available for loop transmission. A loop can operate at only one of the three rates at a given time, hence all Rate Selection Switches of a given loop must be in the same position. However, each loop can operate at any rate, independent of the other loops. The switch positions and their corresponding loop rates are:

Switch Setting	Position	Rates
HIGH	Center	24,000 char./sec.
MED	Down	7,000 char./sec.
LOW	Up	300 char./sec.

4.1.4 ESM Monitor

An ESM monitor is provided and is equipped with lights and switches required for monitoring the operation of the B7* microprocessors. It also provides for direct operator control or intervention of the B7* operation. It can be used with either the NCU B7* or the CIE B7* by plugging it into one of the appropriate card slots provided (see Figure 2-2 and Table 2-1).

The controls (see Figure 4-2) and their functions are as follows:

1. Toggle Switches 1 through 12 – used to manually "toggle-in" a single instruction. Up position represents a binary 1, Down position represents a binary 0. (See B7* List of Instructions for binary representation of instructions.)

   Note: NCU B7*'s are equipped with PROM memory; hence, this capability is not applicable to the NCU B7*.

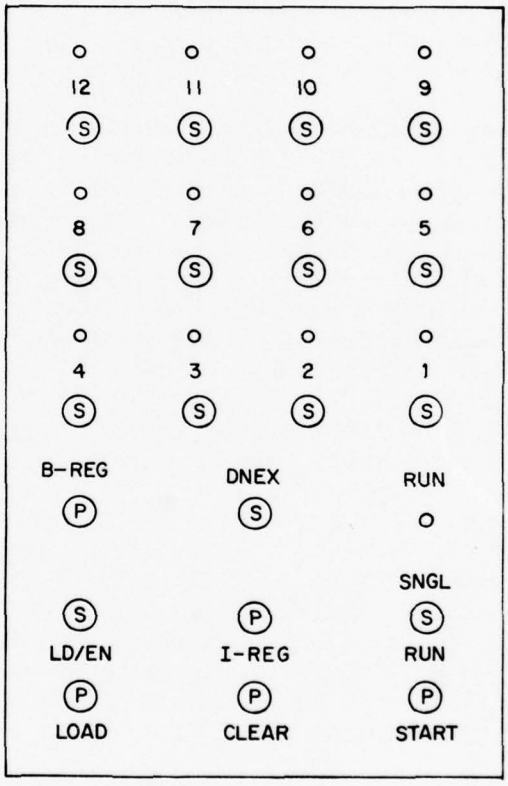
2. Indicator Lights 1 through 12 – Normally display MPCR contents (program address). Other functions are:

   Lights 1-12 = Contents of IR when I-REG button is depressed.

   Lights 1-8 = Contents of B-register when B-REG button is depressed.

3. B-REG Pushbutton – When depressed gates contents of B-Register to Indicator Lights 1-8.

4. I-REG Pushbutton – When depressed gates contents of I-Register to Indicator Lights 1-12.



Legend:

- O Indicator Light
- (S) Toggle Switch-Two Position
- (P) Pushbutton Switch - Momentary

Figure 4-2. ESM Monitor Control Panel

5. RUN Indicator Light – When on, indicates that the B7* is in the Run Mode. When off, B7* is either in the Single Step Mode, or is experiencing a Hard Interrupt.

6. LD/EN Toggle Switch – In the Up position, access to the control memory is enabled, thereby permitting the entry of an instruction from the Toggle Switches 1 through 12. The switch must be in the Down position to read the contents of a memory location (via depressing the I-REG pushbutton).

7. DNEX Toggle Switch – In the Up position (DNEX), the contents of the Instruction Register are held cleared to zero, thereby prohibiting execution of instructions. Note, however, that all zeros in the IR represent the real instruction DEV 0 = 0 and this instruction is used in the system to Soft Interrupt the NCU B7*. Hence, that condition is active in the DNEX position.

8. SNGL/RUN Toggle Switch – In the Up position the B7* can be single-stepped via the START pushbutton - one instruction per depression of the START pushbutton. Note, however, that each instruction stops one clock short of completion. Thus, after a BEX instruction the bits in the B-Register are shifted one bit to the left. Therefore, one more succeeding instruction must be executed before the result in the B-Register is valid. However, if the succeeding instruction involves the B-Register, the bits will again be offset.

   When switched to the RUN position, the START pushbutton must be depressed to initiate the Run Mode.

9. LOAD Pushbutton – Active only when the LD/EN switch is in the Up position. When the LOAD pushbutton is depressed it strobes the instruction as set on Toggle Switches 1-12 into the control memory location indicated on Indicator Lights 1-12. After loading an instruction in this manner, it should always be verified by setting the LD/EN switch to the Down position and depressing the I-REG pushbutton. The instruction then appears on Indicator Lights 1-12.

10. CLEAR Pushbutton – When depressed clears the MPCR to zero. Indicator Lights 1-12 are extinguished. If the B7* is in the Run Mode the program is restarted.

11. START Pushbutton – If the SNGL/RUN switch is in the RUN position, program execution is started. If in the SNGL position, the instruction is executed up to the last clock pulse and the MPCR is incremented.

4.2 ESM SYSTEM TAPES

The ESM system software is contained on four TU10 Magtapes. The contents of these tapes are described below:

4.2.1 Tape #1 - User Language

This tape contains the user language task (.TSK), FORTRAN source files (.FOR) and object files (.OBJ), overlay description language file (.ODL), listing command file (.CMD), and message, system and ATEC files used by the user language program as well as programs used to generate these files. Demo programs PROC1, PROC5, RCMV1, and RCMV5 also are on Tape #1.

4.2.2 Tape #2 - CIE Microcode

This tape contains the microcode source (.DAT) and object (.OBJ) files used for loading the eleven B7* CIE's. The microcode loader utility (ESMLDR) task, source and object file are also on this tape.

4.2.3 Tape #3 - MDMPL Assembler

This tape contains the task, source, object, and overlay description language files for the MDMPL assembler.

4.2.4 Tape #4 - Diagnostics

This tape contains the ESM Diagnostic Library.

4.2.5 Tape Transfer Operations

Files are moved from tape to disk using the FLX utility program. The following FLX tape to disk commands should be used.

Moving Tasks

```
FLX DK0:/CO = MT0: [20,20] USRLN5/BL:98.
```

where the value following BL: is the number of contiguous blocks required.

Moving Microcode Object Files

```
FLX DK0:/FB:256. = MT0: [1,4] LPCKO.OBJ
```

Moving Microcode Source Files - In card Image Mode for Compilation and Message Files

```
FLX DK0:/FA:80. = MT0 [1,4] PDP.DAT
```

Moving all other Files

FLX DK0:/RS = MT0: [20, 20] P0000. FOR/DO

To Obtain a Tape File Directory Listing

FLX CL0: = MT0 [*, *] *. */LI

Tape file directory listings are given in Appendix A.

4.3 SYSTEM START-UP

The following procedures should be used when starting up the ESM.

1. Power-up PDP-11 Host Processors per PDP-11 documentation. Power-up the three ESM cabinets and the TD802 terminals by turning on the a-c power switches.

2. Load ESM disk cartridge.

3. Bootstrap using octal console address 173030.

4. Enter Time; e.g., TIM 08:05:00 11/22/76. (Steps 4 through 9 are entered from the VT-52 DEC scope.)

5. SET /UIC = [1, 20]

6. RUN [20, 20] ESMLDR

   Load the following object file names (repeat Step 6 for each file loaded):

LOAD SW.	FILE NAME	
HOST	HST1. OBJ	loop #1
G1-2	GAT2. OBJ	
G1-3	GAT3. OBJ	
CRT	CRT4. OBJ	loop #2
HOST	HST5. OBJ	
G2-1	GAT6. OBJ	
G2-3	GAT7. OBJ	
CRT	CRT8. OBJ	loop #3
HOST	HST9. OBJ	
G3-2	GAT10. OBJ	
G3-1	GAT11. O BJ	

Note: CRT4. OBJ and CRT8. OBJ use Host B as Primary Dialogue Director; for Host A Dialogue Director, load CRT4S. OBJ and/or CRT8S. OBJ.

For loading, the right-most switch on top row (LD/EN switch) is placed in Up position. The node to be loaded should have its LOAD switch in the second row (per Figure 4-1) in the up position. Press M-CLR (MASTER CLEAR) button. Occasionally nodes may not load properly, and may require repeating the load procedure. After loading, press second row LOAD switch down and then upper row LD/EN switch down and then depress M-CLR. When all nodes are loaded the RESET switch in each loop is switched up and then back down, and the M-CLR button in each loop is depressed to initialize the system. The user language is then initiated by the following steps:

7. SET /UIC = [20,20]

8. @STESM (wait for display of "@ <EOF>", before proceeding to Step 9).

9. RUN USRLNG

10. The user language is initiated from a remote CRT (in loops 2 and 3) by transmitting some character(s) (e.g., BEGIN). The system. will then prompt for user code and then password for which the user can respond with any transmission.

Characters are entered on the CRT when it is in the LOCAL mode. Characters are transmitted from the upper-left-hand corner of the screen to the cursor location. A maximum of three lines of data can be transmitted at once as a packet. Characters are transmitted by depressing the TRANSMIT key on the upper-right-hand corner of the keyboard. The terminal will normally go into receive mode within 2 seconds after the transmit key has been depressed. If this fails to occur, reenter LOCAL Mode and then redepress the TRANSMIT key. If a message is to be received and the CRT is in LOCAL mode, the terminal will beep and the ENQ light will be on until the operator presses the RECEIVE key. The audible beeping can be disabled by turning the associated volume control to the extreme right.

The STESM MCR command file is used to load a permanent copy of the system status file which corresponds to the microcode that is loaded. In this manner changes to the system during the course of the day will not be permanent. This command file should also be activated if the system is cleared after changes have been made to the system status file (via mode 3 of the user language).

To abort the user language enter "ABORT" on the ESM TD802 CRT.

To load files from tapes, see Section 4.2.5.

To load and run diagnostics, see Section 4.5.6.

4.4 USER LANGUAGE

The following Host-CRT dialogue is given as an example of the ESM User language illustrating the flow diagrams of Figures 4-3 through 4-8. Note that CRT responses will be typed on the first line of the CRT and that the TRANSMIT key must be pressed for each CRT response. The dialogue may be terminated at any time by entering DS at the CRT.

CRT: * BEGIN

HOST: THIS IS THE ESM - (EXPLORATORY SYSCON MODEL)
ENTER USERCODE PLEASE

CRT: Usercode

HOST: ENTER PASSWORD PLEASE

CRT: Password

HOST: YOU ARE NOW LOGGED IN - (TO LOGOUT, ENTER"DS")
PLEASE SELECT ONE MODE OF OPERATION:
1. CRT TO CRT.
2. SYSTEM INQUIRY.
3. SYSTEM CONTROL.
4. FILE ACCESS.
5. CARD FORMAT.

CRT: 1 - 5

4.4.1 Mode 1 CRT-to-CRT (See Figure 4-4)

HOST ENTER DEST CRT NODE DESIGNATOR (ND) - 4 FOR LP#2, 8 FOR LP#3. IF NOT KNOWN ENTER "NDI"

CRT: 4, 8

HOST: PLEASE TYPE IN MESSAGE AND TRANSMIT

CRT: The message. (Enter on first 3 lines of CRT.)

HOST: PLEASE SELECT ONE MODE OF OPERATION:
1. NEW MESSAGE TO SAME CRT.
2. NEW MESSAGE TO ANOTHER CRT.
3. LOGOUT.
4. NEW MODE OF OPERATION.

CRT: 1 - 4

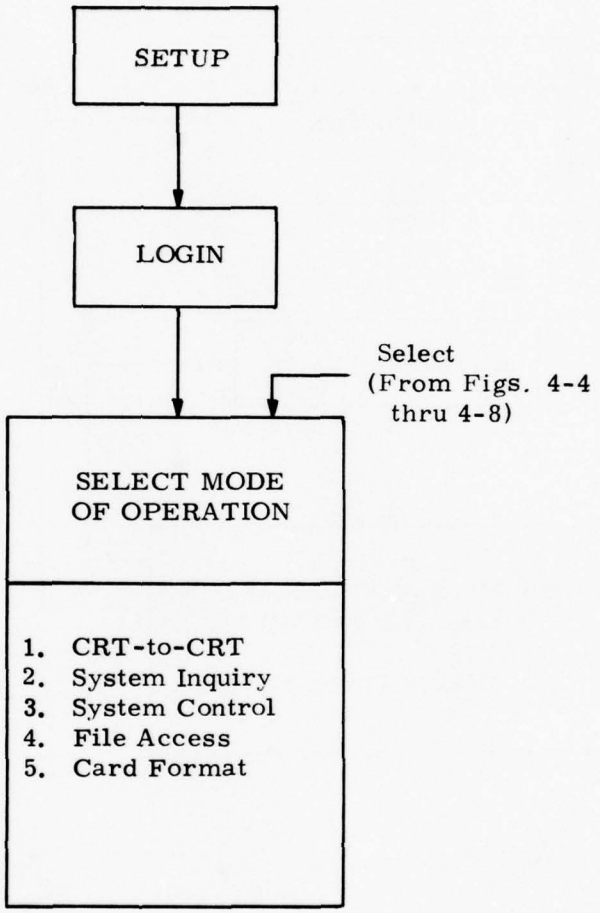


Figure 4-3. ESM User Language

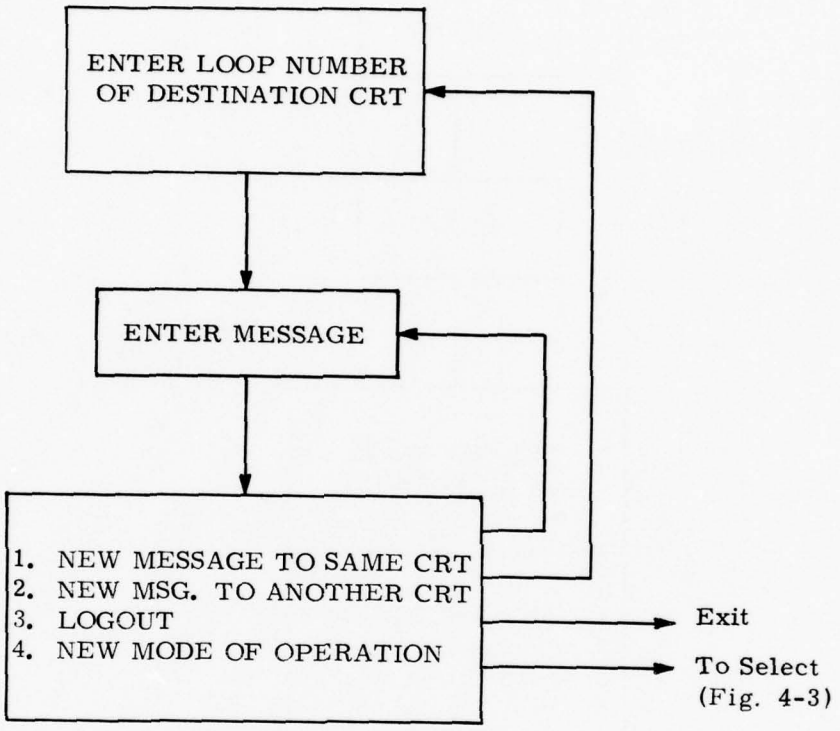


Figure 4-4. CRT-to-CRT Mode of Operation

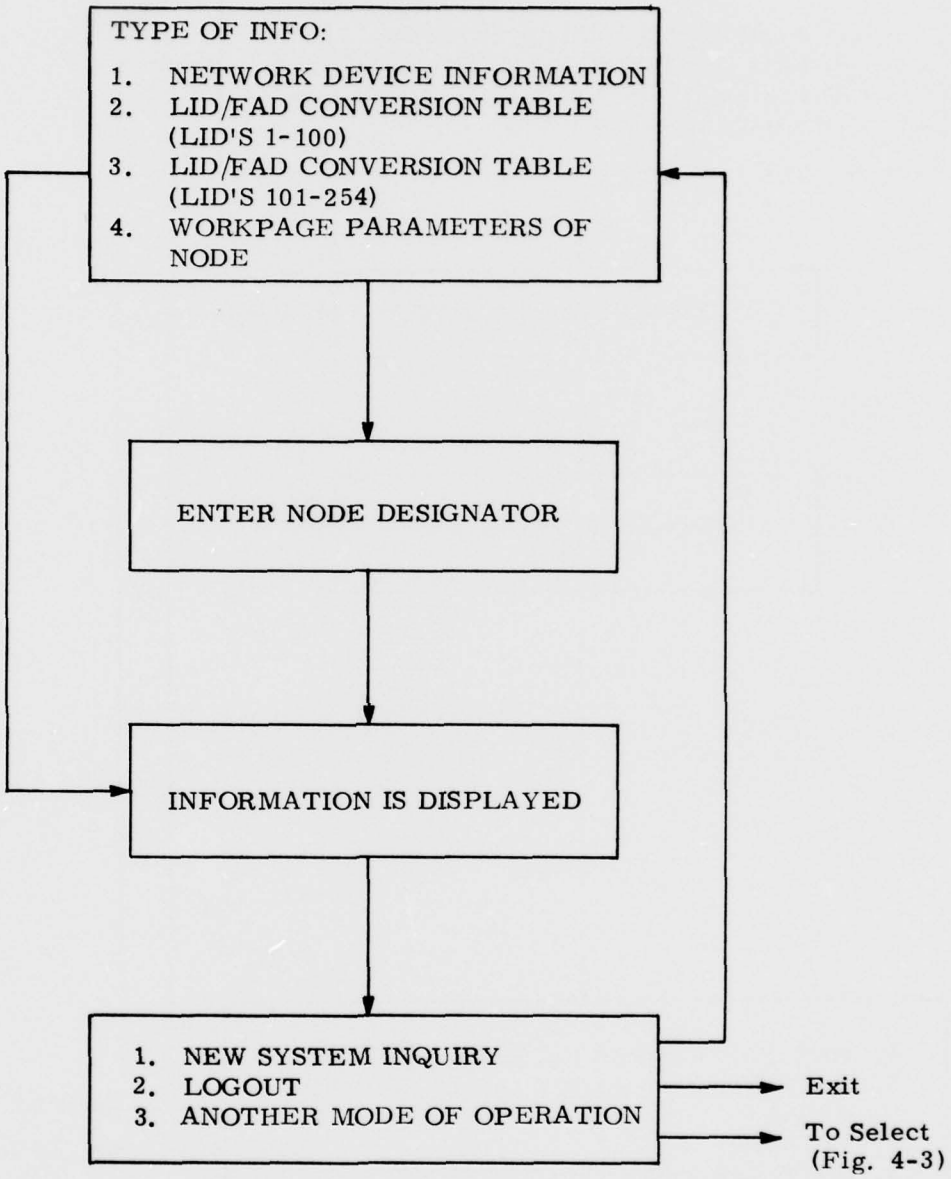


Figure 4-5. System Inquiry Mode of Operation

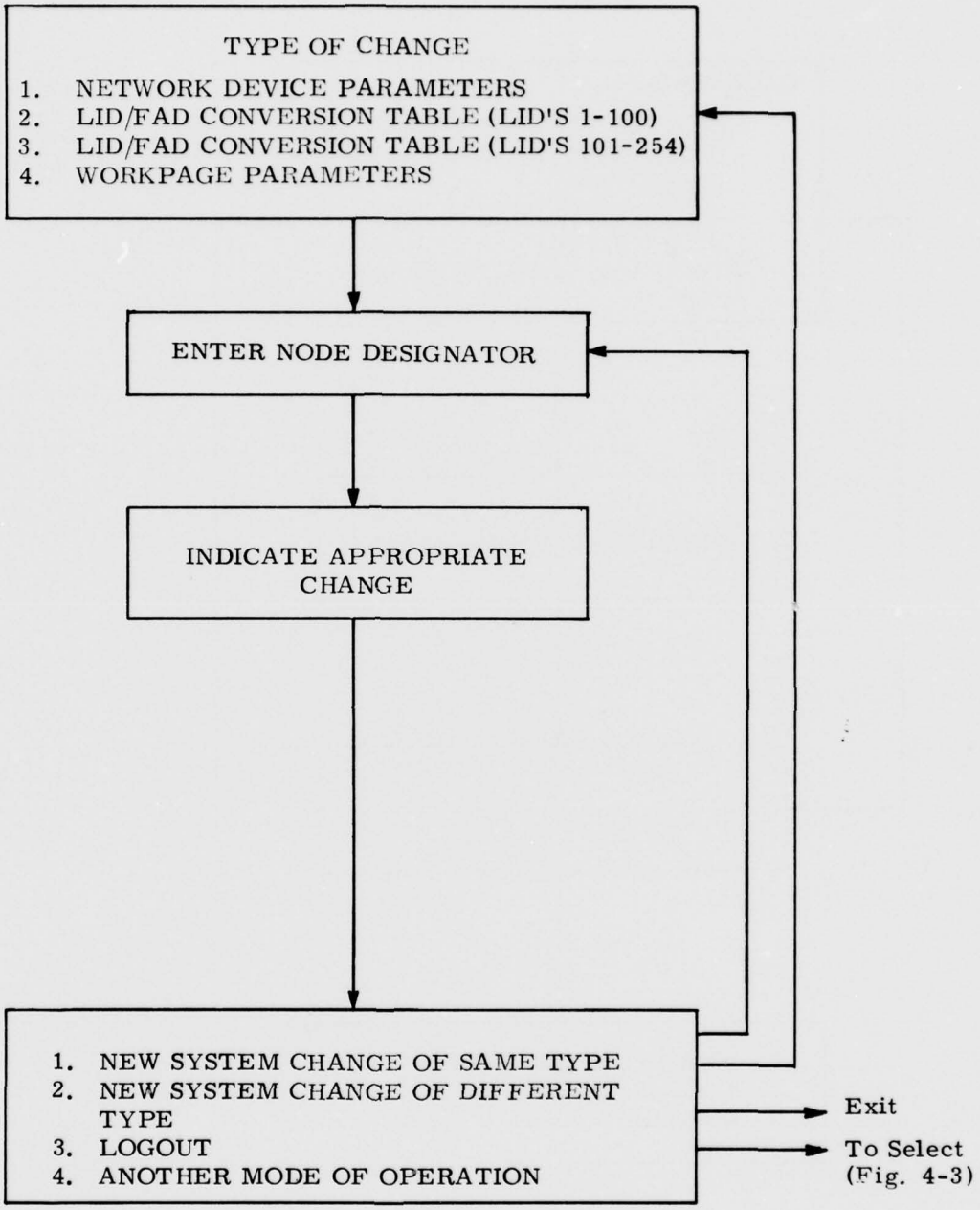


Figure 4-6. System Control Mode of Operation

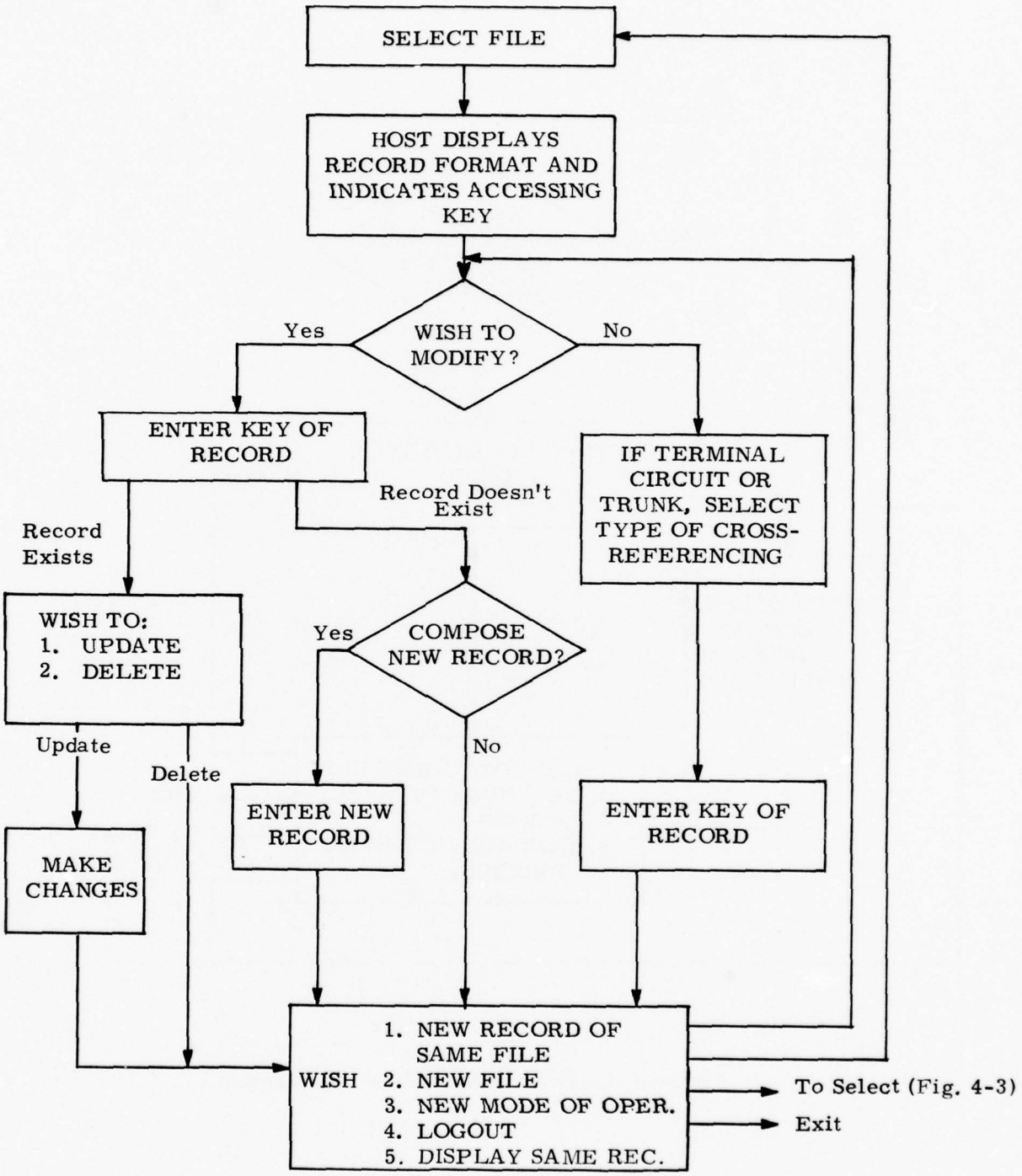


Figure 4-7. File Access Mode of Operation

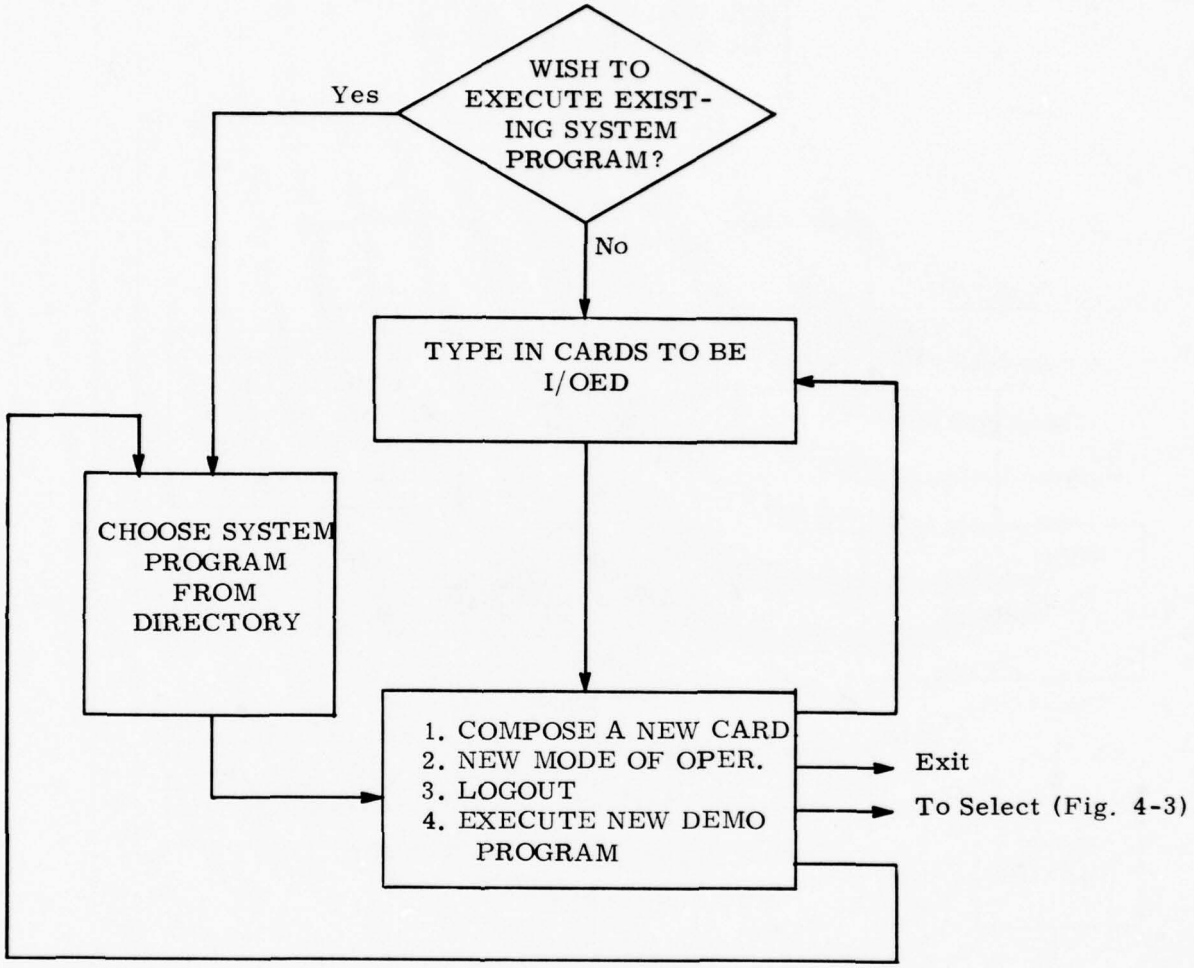


Figure 4-8. Card Format Mode of Operation

Dialogue now repeats as shown in Figure 4-4. If 3 is chosen, then

HOST: YOU ARE LOGGED OUT FROM ESM.

4.4.2 Mode 2, System Inquiry (See Figure 4-5)

HOST: PLEASE SELECT TYPE OF SYSTEM INFORMATION:
1. NETWORK DEVICE INFORMATION.
2. LID/FAD CONVERSION TABLE (LID'S 1-100)
3. LID/FAD CONVERSION TABLE (LID'S 101-254)
4. WORKPAGE PARAMETERS OF NODE.

*CRT: 1 - 4

HOST: (If 1): See Figure 4-9 for typical display.

HOST: (If 2 - 4): PLEASE ENTER NODE DESIGNATOR (ND). IF ND IS NOT KNOWN, ENTER NDI FOR NETWORK DEVICE INFORMATION.

CRT: Node designator or "NDI".

HOST: Typical display is shown in Figures 4-9 through 4-12. Figure 4-9 results from "NDI" or from response 1 at * above. Figure 4-10 is shown for response 2 at * above; Figure 4-11 results from response 3 at *; Figure 4-12 results for response 4 at *.

To continue after display, press transmit key.

HOST: PLEASE SELECT ONE OF THE FOLLOWING:
1. NEW SYSTEM INQUIRY.
2. LOGOUT.
3. ANOTHER MODE OF OPERATION.

CRT: 1 - 3

4.4.3 Mode 3, System Control (See Figure 4-6)

*HOST: PLEASE SELECT TYPE OF SYSTEM PARAMETERS TO BE CHANGED.
1. NETWORK DEVICE PARAMETERS.
2. LID/FAD CONVERSION TABLE (LID'S 1-100)
3. LID/FAD CONVERSION TABLE (LID'S 101-254)
4. WORKPAGE PARAMETERS. (NOT YET IMPLEMENTED IN CIE MEMORY)

NETWORK DEVICE INFORMATION

LOCAL LOOP

	LOOP 1			LOOP 2			LOOP 3		
NT	ND	RDA	WTD	ND	RDA	WTD		RDA	WTD
CRT	-	-	-	4	4	2	8	4	3
HOST	1	1	3	5	2	1	9	3	2
GATE#2	2	2	1	6	1	3	10	2	1
GATE#3	3	3	2	7	3	4	11	1	4

NOTE: NT IS NODE TYPE, ND IS NODE DESIGNATOR, RDA IS READ ADDRESS AND WTD IS WRITE TOKEN DESTINATION.

PRESS "XMT" KEY FOR NEXT INSTRUCTION.

Figure 4-9. Typical CRT Display for Network Device Information

LID/FAD CONVERSION TABLE

1 1 1 4 2 1 3 3 3 3 3
0
0
0
0

Figure 4-10. Typical CRT Display for Logical ID's by Node

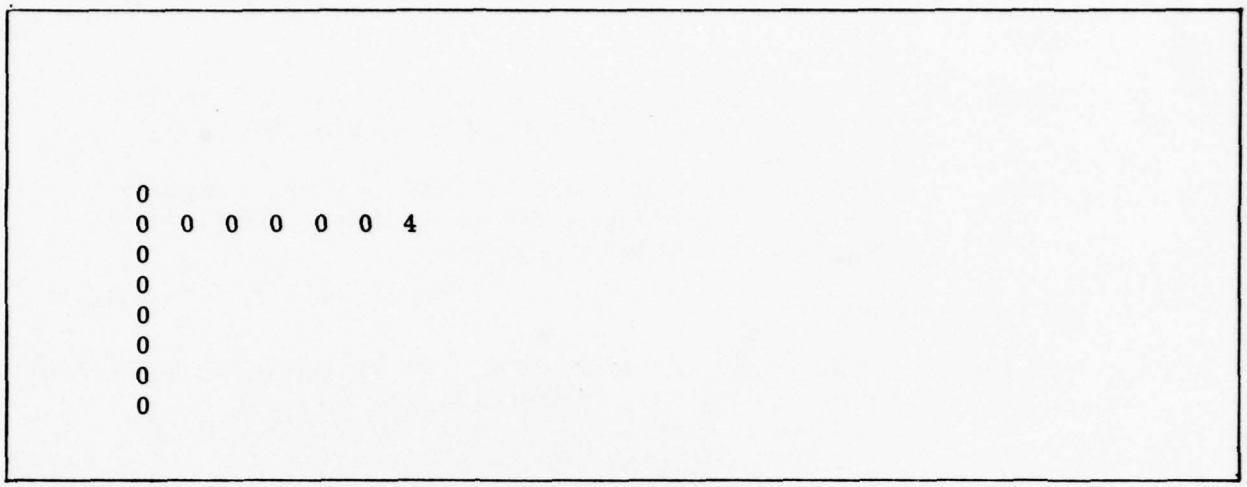


Figure 4-11. Typical CRT Display for Logical ID/Functional Address Table

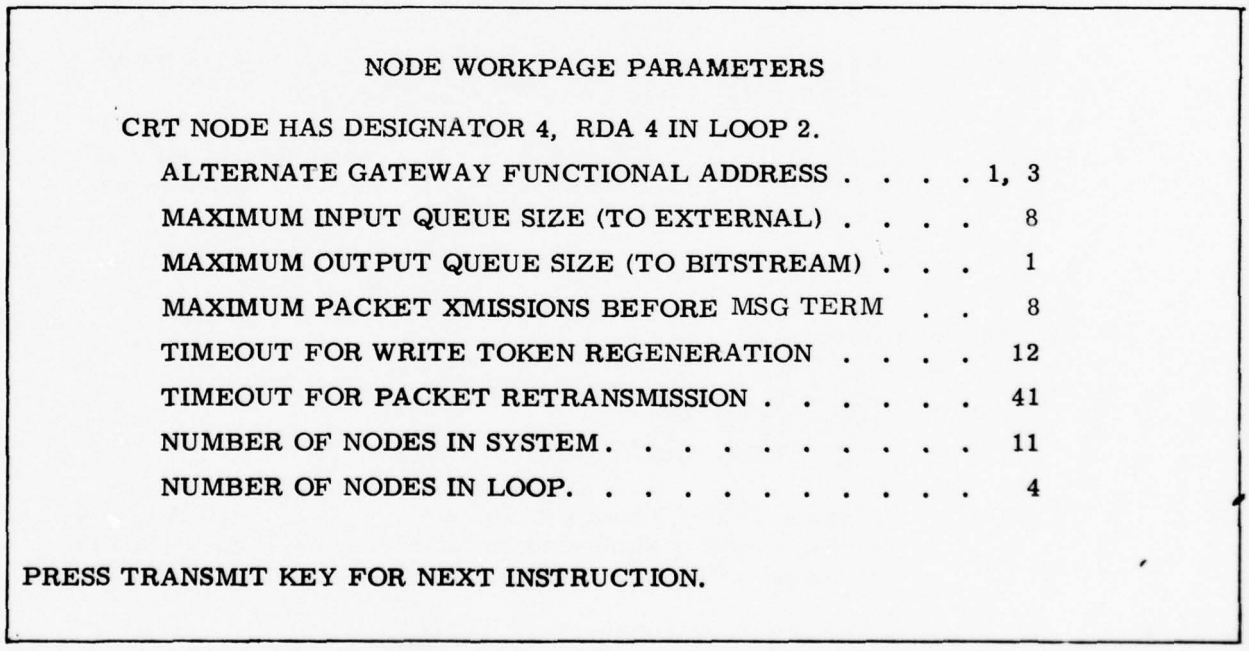


Figure 4-12. Typical CRT Display for Node Workpage Parameters

CRT: 1 - 4

HOST: PLEASE SELECT NODE DESIGNATOR (ND) AND ENTER
IF ND IS NOT KNOWN, ENTER "NDI" FOR DISPLAY.

CRT: Node designator or "NDI". (If "NDI" is given, a display similar to that of Figure 4-9 will be shown. Then pressing XMT key returns to HOST above).

If 1 at * was selected.

HOST: PLEASE SELECT PARAMETER TO BE CHANGED, FOLLOWED BY THE NEW VALUE. (FORMAT I1, I3, 5X)
1. NODE DESIGNATOR. -- NOT IMPLEMENTED
2. FUNCTIONAL ADDRESS.
3. WRITE TOKEN DESTINATION.
4. NO CHANGE

CRT: 1 - 4 Value

(Go to ** for next host entry.)

If 2 at * was selected.

HOST: PLEASE ENTER LID FOLLOWED BY NEW FAD (FORMAT I4, I4)
FOR TABLE PAGE DISPLAY, ENTER "LID".

CRT: LID, FAD OR "LID". (If "LID" is given, a display similar to that of Figure 4-10 will be shown. Pressing XMIT key returns to HOST above.)

(Go to ** for next host entry.)

If 3 at * was selected.

HOST: PLEASE ENTER LID FOLLOWED BY NEW FAD
FORMAT (I4, I4)
FOR TABLE PAGE DISPLAY, ENTER "TAB".

CRT: Logical ID New Functional Address or "TAB". (If "TAB" is given, a display similar to that of Figure 4-11 will be shown. Pressing XMT key returns to HOST above).

(Go to ** for next host entry).

If 4 at * was selected

HOST: PLEASE ENTER ONE OF THE FOLLOWING FOLLOWED BY NEW VALUE. (FORMAT I1, A7) FOR NODE WKPG DISPLAY, ENTER "NNWD":

1. ALTERNATE GATEWAY FUNCTIONAL ADDRESS.
2. ALTERNATE GATEWAY FUNCTIONAL ADDRESS.
3. MAXIMUM INPUT QUEUE SIZE (EXTERNAL).
4. MAXIMUM OUTPUT QUEUE SIZE (BITSTREAM).
5. MAXIMUM PACKET XMISSIONS BEFORE MSG. TERM.
6. TIMEOUT FOR WRITE TOKEN REGENERATION.
7. TIMEOUT FOR PACKET RETRANSMISSION.
8. NUMBER OF NODES IN SYSTEM.
9. NUMBER OF NODES IN LOOP.

CRT 1 - 9 New Value or "NNWD". (If "NNWD" is given, a display similar to that of Figure 4-12 will be shown. Pressing XMT key returns to HOST above.)

HOST: PLEASE SELECT ONE OF THE FOLLOWING:

1. NEW SYSTEM CHANGE OF SAME TYPE.
2. NEW SYSTEM CHANGE OF DIFFERENT TYPE.
3. LOGOUT.
4. ANOTHER MODE OF OPERATION.

CRT: 1 - 4

Note: System control changes can cause malfunction of the system if care is not exercised. Certain types of malfunctions may be simulated through suitable system control changes. An example is a suitable change in functional address of a node such that the node will no longer receive messages.

4.4.4 Mode 4, File Access (See Figure 4-7)

HOST: PLEASE SELECT FILE TO BE ACCESSED: (ONLY #1-4 ONLY ON DISK):

1. LOCATION FILE.
2. CIRCUIT DIRECTORY.
3. TRUNK DIRECTORY.
4. TERMINAL DIRECTORY.
5. SATELLITE DIRECTORY.
6. SUBSTANDARD CIRCUITS.
7. MESSAGE FILE.
8. SUBSCRIBER LIST.
9. INSTALLATION LIST.
10. TRAFFIC REPORT FILE.

CRT: 1 - 10.

HOST: A RECORD OF THE FILE YOU HAVE SELECTED HAS THE FOLLOWING FORMAT:

Format Display.

THE KEY HAS A (Value) CHARACTER CODE IN FORM (ALPHABETIC, NUMERIC, ALPHANUMERIC)

DO YOU WISH TO MODIFY THIS FILE?

1. YES.
2. NO.

CRT: 1 - 2

If 1 is selected above, to to *.
If 2 is selected and file selection was 1, go to **.
If 2 is selected, and the file selection was 2 or 3.

HOST: THE 2 BYTE ALPHANUMERIC LOCATION KEY OF THE CIRCUIT OR TRUNK DIRECTORY FILES MAY BE USED AS A KEY TO CROSS-REFERENCE THE TERMINAL DIRECTORY FILE. DO YOU WISH TO CROSS-REFERENCE?
1. YES.
2. NO.

CRT: 1 - 2 Go to **

If file selection was 4,

HOST: THE 2 BYTE ALPHANUMERIC LOCATION KEY OF THE TERMINAL DIRECTORY FILE MAY BE USED AS A KEY TO CROSS-REFERENCE THE CIRCUIT DIRECTORY AND/OR TRUNK DIRECTORY FILES. PLEASE SELECT MODE OF ACCESS:
1. NO CROSS-REFERENCE.
2. CROSS-REFERENCE CIRCUIT DIRECTORY.
3. CROSS-REFERENCE TRUNK DIRECTORY.
4. CROSS-REFERENCE BOTH.

CRT: 1 - 4

** HOST: PLEASE ENTER ACCESS KEY.

CRT: KEY

HOST: (If key is valid and record exists, displays record.)
(If key does not exist, requests new key.)

CRT: Press XMT key. Go to ***.

* For record modification

@ HOST: PLEASE ENTER KEY OF RECORD TO BE MODIFIED.

CRT: Key

If record exists, record is displayed.

HOST: FOR THIS RECORD, PLEASE SELECT TYPE OF DESIRED CHANGE:
1. UPDATE.
2. DELETE.

CRT: 1 - 2. If 2 go to @@

If 1, record to be updated.

HOST: MAKE ANY CHANGES YOU WISH USING CRT KEYBOARD.
WHEN CHANGES ARE COMPLETE, PRESS XMT KEY.
ENTER UPDATED RECORD ON FIRST LINE OF CRT.
(Record is entered on first line of CRT - fill entire line with spaces or tabs for formatting.)

CRT: Edits and transmits. Go to @@

If record does not exist,

HOST: THE RECORD DOES NOT EXIST. DO YOU WISH TO ADD A RECORD TO THE FILE?
1. YES
2. NO

CRT: 1 - 2. If 2 go to @@

If 1, record to be added.

HOST: Give record format.
KEY IS (X) CHARACTERS OF TYPE (type).
ENTER THE RECORD ACCORDING TO THE ABOVE FORMAT.
WHEN RECORD IS COMPLETE, PRESS XMT KEY.
ENTER NEW RECORD ON FIRST LINE OF CRT.
(Center on first line of CRT - fill line with spaces or tabs for formatting.)

CRT: Edits and transmits.

@@HOST: MODIFICATION COMPLETE. (Record unlock occurs.)

***HOST: PLEASE SELECT ONE OF THE FOLLOWING:
1. NEW RECORD OF FILE.
2. NEW FILE.
3. NEW MODE OF OPERATION.
4. LOGOUT.
5. DISPLAY SAME RECORD.

(Dialogue repeats as shown in Figure 4-7).

4.4.5 Mode 5, Card Format (See Figure 4-8)

HOST: DO YOU WISH TO EXECUTE AN ESM DEMONSTRATION PROGRAM?
1. YES.
2. NO.

CRT: 1 - 2

If 1 was selected,

HOST: PLEASE SELECT PROGRAM TO BE EXECUTED. USE CRT AS AN I/O DEVICE FOR THE PROGRAM.
1. CRT BROADCAST.
2. RECORD MOVE.
3. INTERPROCESS COMMUNICATION - ABORT USRLNG, RUN PROC
. .
. .
. .

CRT: Selection. Return to * will be automatic after program run.

If 2 was selected,

HOST: YOUR CRT WILL NOW ACT AS A USER TERMINAL INPUT TO A HOST PROCESSOR. PLEASE ADHERE TO STANDARD CONTROL FORMAT.

CRT: Transmit control deck and acts as user terminal. When a user program ends, return to the ESM system may be initiated by card format to be developed.

*HOST: PLEASE SELECT ONE OF THE FOLLOWING:
1. NEW CARD FORMAT RUN.
2. NEW MODE OF OPERATION.
3. LOGOUT.
4. NEW DEMO PROGRAM.

4.5 MAINTENANCE AND DIAGNOSTICS

The maintenance and diagnostics described in this section are those which may be performed by user personnel. However, it is assumed that these personnel are familiar with the ESM to the extent described in this manual. These maintenance activities include:

1. Cleaning of filters,
2. Replacement of fuses,
3. Verification of proper operation via successful running of diagnostics,
4. Isolation of faulty PC Boards via running of diagnostics, and
5. Replacement of identified faulty board by a spare PC board.

Maintenance operations will require the removal of one or both side panels. These are lift-off panels, but panel retainer bolts at the bottom of the cabinet must first be loosened sufficiently to permit panel removal.

CAUTION: When performing maintenance on an ESM cabinet, care must be exercised to insure that foreign matter does not fall into the cabinet power supply through the fan or other openings in the top of the power supply. This can best be accomplished by covering these openings when the fan is not operating (i.e., a-c power is removed from the cabinet).

4.5.1 Filters and Fans

Two filters are located in the bottom of each ESM cabinet. These filters are removed by rotating the retainer bar under the filter, tilting the filter and dropping it through the bottom of the cabinet. They should be removed and washed periodically (at least annually).

Fans are mounted at the upper rear of the cabinet and on the top of the cabinet power supply. These fans require no specific maintenance, but should be checked periodically for proper operation. Excessive noise or vibration would indicate a need for fan replacement or retightening of mounting hardware.

4.5.2 Fuse Replacement and Power Supply Checks

Fuses can be replaced readily, but repeated failures can be attributed to more serious faults. Fuses of only the correct size and rating should be used. Fuse sizes and locations are presented in paragraph 4.1.1.

Power supply voltages should be checked periodically (at least semi-annually). These checks should be made on both the backplane and the power supply itself. They include voltage level, ripple,and also balance between both halves of the backplane. Details of these measurements and any adjustments required are provided in the ESM Hardware Maintenance Manual.

4.5.3 Verification of Proper Operation

Proper operation of the ESM hardware can be verified by running the diagnostic programs described in paragraph 4.5.6. That is, if all of the diagnostic routines run successfully, the hardware generally can be assumed to be good. Note, however, that these routines do not check every single function and, therefore, are not totally conclusive. But, they do provide a significant level of confidence of system operability.

4.5.4 Isolation of Faulty PC Boards

The existence of a fault in the ESM generally can be located by running the Diagnostics as described in paragraph 4.5.6. That is, the fault can be isolated to a Terminal, a Host, or one or more PC boards in any of the ESM cabinets. The suspected

element can then be further verified by substituting a good element for the suspected element. For example, one CRT terminal can be substituted for another by moving the cable connector at the CRT end. Also, a spare PC Board may be substituted for a suspected faulty board in any of the three ESM cabinets (see para. 4.5.5), and after substitution the diagnostic(s) can be rerun to verify proper operation.

4.5.5 Replacement of a Faulty PC Board

Replacement of PC Boards is limited to those contained in the three ESM cabinets. A suspected faulty board in any of these cabinets can be replaced by a spare board of the same type, or by a board currently not being used in one of the other cabinets. As a precaution relative to accidentally causing an instruction to be changed in CIE Control memory, the associated node should be placed in the DNEX state while removing or inserting a PC Board. For PC Board locations and complete identifications, refer to Figure 2-2 and Table 2-1, respectively.

4.5.6 Loading and Running Diagnostics

This section presents the procedures for loading and running the diagnostic programs supplied with the ESM. Those programs provide the capability to verify proper operation of the ESM or to verify that a fault exists. They also permit isolation of a fault to a specific hardware element (see preceding paragraph 4.5.4). The flow charts and code listings for these programs are provided separately and should be referred to for a thorough understanding of the use and capabilities of these programs.

The procedure for loading the diagnostic(s) is as follows:

1. Mount Diagnostic Tape on Tape Transport of Host Processor B (connected to Loop 2).

2. At DECscope, do the following:

   - Set User Identification code to Access File by entering
     SET /UIC = [1, 4]
   - Move object file to disk. FLX DK0:/FB:256. = MT0: [1, 4] name. OBJ
   - Load object file into suspect node(s)' CIE's.
     RUN [20, 20] ESMLDR
     Enter filename.

3. At ESM cabinet:

   - Set LD/EN Switch to Up position
   - Set Selected Node LOAD Switch to Up position
   - Depress M-CLR pushbutton.

4. At DECscope: Press Carriage Return key to initiate loading.

   Note: It is possible to load nodes in different loops simultaneously but not nodes within the same loop.

5. At appropriate ESM cabinet and node:

   - Reset Node LOAD Switch (Switch Down)
   - Reset LD/EN Switch (Switch Down)
   - Run diagnostic using ESM Monitor.

   Note: When loading with Monitor plugged-in, the Monitor should be in the RUN mode with RUN light on. (See para. 4.1.4).

The following paragraphs identify the various diagnostic programs and describe their application to the ESM:

1. Memory Checking Program

   Source file MEMCK.DAT
   Object file MEMCKO.OBJ

   Purpose: For checking NCU and CIE data memory boards.

   Description: The bit patterns 10101010, 01010101 and sequential numbers are written into memory and read out again for all NCU and CIE memory pages. If all checks pass the program hangs at location NOERR. If there is an error in the NCU data memory the program hangs at NCUERR. If there is an error in the CIE data memory the program hangs at CIEERR. The operator may then single step the program to find the word and page number where the test failed and examine the contents of the bad page. There are a total of 44 CIE pages, 16 each on the first two CIE memory cards and 12 on the third card. Thus, a failure on page 16 would indicate a problem on the second data memory card.

2. Block Transfer Diagnostic

Source file BLKS.DAT
Object file BLOUT.OBJ

Purpose: For checking memory reading and writing and block transfers between NCU and CIE ancillary boards.

Description: This program loads page 0 of the NCU with sequential numbers, reads them from the CIE and then block transfers page 0 of the NCU to page 3 of the CIE. The result of the transfer is then read and the program hangs at location NG1 on failure to read sequential numbers. The program then loads CIE page 6 with sequential numbers, reads the data and then block transfers to page 2 of the NCU. The result of the transfer is then read and the program hangs at location NG2 on failure. The program hangs at HANG5 if there are no failures.

Special Instructions: The NCU must be in a "DON'T EXECUTE" state so that it may not modify its data memory.

3. Gateway Debug Diagnostic

Source file GTB.DAT
Object file GTBO.OBJ

Purpose: To check gateway interfaces between two cabinets.

Description: The program is loaded into gateway nodes in two loops. One gateway sends sequential numbers to the other gateway which reads the result. The sending gateway loads CIE page 0 with sequential numbers, sends the page across the interface and then may read the original page, if required. The reading gateway code starts at octal location 40. It block transfers the output buffer contents to CIE page 1 and reads the results.

4. CRT-to-CRT Via Gateway Diagnostic

Source files	CTCC.DAT
	CTCG.DAT
Object files	CTCCO.OBJ
	CTCGO.OBJ

Purpose: For checking in loops #2, #3 gateway interface, partial loop (node) verification, and CRT interfaces.

Loading Instructions: Object file CTCCO.OBJ is loaded into CRT nodes on loops #2, 3. Object file CTCGO.OBJ is loaded into gateway node GB in loop #2, and gateway node GA in loop #3. Put other nodes into DNEX and CLEAR state via panel-mounted switches while running diagnostic.

Description: These programs accept a packet from a CRT, send the packet via the loop to a gateway node, transfer the packet across the interface, and then deliver the packet to the CRT via the loop. After hitting the master clear and loop clear, acceptable operation allows a packet to be transmitted from one CRT to the other CRT connected to the other loop. Messages may be sent in either direction. A terminal that is in local mode will beep when there is a packet to be received.

5. CRT Interface Diagnostic

Source file CRTCK.DAT
Object file CRTOBJ.OBJ

Purpose: For checking CRT interface boards and TD802 CRT operation.

Description: This program accepts a packet from the CRT and then resends the packet back to the CRT preceded by 7 line feeds. The operator types a packet (up to 3 lines), transmits the packet and proper operation results in the packet being displayed on the bottom part of the screen.

6. PDP-11 Interface Diagnostic

PDP-11 files: Source PDP.FOR
Object PDP.OBJ
Task [1,4] PDP.TSK

CIE files: Source PDP.DAT
Object PDPO.OBJ

Loading: Load the PDP-11 connected CIE's with PDPO.OBJ. Run the CIE connected B7*. Run the task on the PDP-11 to be tested; i.e., RUN [1,4] PDP.TSK.

Purpose: This program checks the M1710 PDP-11 interface and the Host Interface Board. A three-line-packet is entered on the DECWRITER. The CIE hangs (at HNG1) after receiving the packet, and memory page 20 can be examined by single-stepping. The packet may then be written back to the DECWRITER by running the program from location WRTB.

7. Loop Check Diagnostic

Source file LPCK.DAT
Object file LPCKO.OBJ

Purpose: For checking reading and writing ability of Loop Interface boards, loop operation, and Clock-Retimer operation.

Description: This program contains the code for writing a packet of sequential numbers to the loop and for reading the packet from the loop. For a successful read the program hangs at location NOERR. For an unsuccessful read the program hangs at location ERROR where the word location and data of the bad read can be examined.

Operating Procedures: For each loop, one node is designated the writer and one node the reader. For the writer, toggle in two STEP (hex 187) instructions at octal addresses 16 and 17. Put other two nodes into DON'T EXECUTE, CLEAR state. To run the test, clear the loop, clear the reader, and then clear the writer. The reader will then halt at location ERROR or NOERR depending on the outcome of the test.

4.6 MICROCODE ASSEMBLER

The eleven B7* CIE microprocessors are loaded with microcode object files that are stored on the PDP/11 processor connected to loop #2. The object files consist of records made up of 128 twelve-bit microinstructions. An MDMPL assembler written in FORTRAN is provided with the ESM for microcode creation or modification. The Mini-D Microprogramming Language (MDMPL) is described in the Software Maintenance Manual. Microcode source files can be created or edited using the RSX11M Editor Utility (EDI).

An MDMPL source file has the following format:

First line	$12BIT (begins in column 7)
Second line	PROGRAM-ID name. (begins in column 8)
Value statements	(Starting in column 8)
Program statements	(Begin in column 15)
Last statement	END?. (Begin in column 15)
Comments	*Comment (Begin in column 7).

Statements are always terminated by a period. Labels start in column 8 and terminate with a period. Labels can consist of up to 7 alphanumeric characters and may not contain embedded assembler reserved words, e.g., EXT, LC1, LST, MST, AOV, IF, STEP, SKIP, ELSE. Statements may not start at or before column 8, and by convention start at column 15. Comments following statements, by convention, start at column 40. An asterisk, *, in column 7 indicates a comment card.

After the file is edited using the EDI Utility, it must be put into fixed record, 80-character, formatted ASCII card images for input to the MDMPL assembler. This can be done by writing the file to tape, and then back again to disk using the file transfer (FLX) utility, e.g.:

```
FLX MT0:/DO = DK0 [1,4] file-name.DAT/RS

FLX DK0:/FA:80. = MT0: [1,4] file-name.DAT
```

FLX and EDI commands are given in the RSX11M Utilities Procedures Manual.

When the source file is properly formatted on disk (latest version), run the MDMPL assembler by entering RUN [20, 20] MDMPL on the DECSCOPE. The program will prompt for the source filename and object filename. By convention, source microcode files are of type DAT, and object microcode filenames are of type OBJ. Default conditions allow for program listing with possible error messages on the DECSCOPE. Output may be stopped by entering control C, and it may be resumed by hitting the return key. For a hard copy printout enter RED TT0: = TT1: before running MDMPL. The number of errors is printed at the end of the program.

Table 4-1 gives a list of instruction functions provided by the nodal ancillary logic.

Table 4-1. CIE Instruction Functions

Instruction	Function
OUT0 = < word address expression >.	Set Word Address (0-255)
OUT1 = < page address expression >.	Set Page Address (0-43)
OUT2 = < expression >.	Write Value of expression to data memory
OUT3 AMPCR = AMPCR.	Reset EXT
BEX0 B = B.	Exodevice Status Register Contents moved to B Register.
BEX1 A1 = A1.	Move memory contents to B register
BEX2 A2 = A2.	Send output buffer status to exodevice
BEX3 A3 = A3.	Move clock register value to B register
DEV1 = 0.	Clear DEV's, enable auto-incrementing of memory address register
DEV1 = 1.	Terminate Block Transfer
DEV1 = 2.	EX0 to CIE Block Transfer
DEV1 = 4.	CIE to EX0 Block Transfer
DEV1 = 80.	NCU to CIE Block Transfer
DEV1 = 96.	Access NCU Data Memory
DEV1 = 104.	CIE to NCU Block Transfer
DEV1 = 128.	Disable auto-incrementing of memory address register
DEV0 = 1.	Interrupt NCU (Soft-Set NCU's EXT)
DEV2 = 1.	Send Input Buffer status to Exodevice
DEV3 = 1.	Interrupt NCU (Hard-Set NCU's MPAD = 0).

Timing and other constraints define a set of rules for the above instructions:

1. By convention a BEX1 A1 = A1 instruction is preceded by an A1 = A1 instruction.

2. An OUT2 instruction must be followed by a STEP instruction.

3. An OUT3 instruction must be done twice.

4. The CIE memory address register may not be set to location 255 when NCU data memory is to be accessed.

5. Incrementing the NCU memory address register under CIE control also increments the CIE memory address register.

6. The CIE must release NCU data memory by the DEV1 = 0 instruction before the NCU can access its data memory under NCU control.

Since the CRT interfaces have a low speed (9600 baud), CIE-EXO block transfers are not necessary. Thus, for CRT-connected CIE's the above CIE-EX0 transfer instructions send a byte at a time rather than a 256 byte block transfer as is done for Gateway and Host connected CIE's.

The following program segments illustrate the use of the above instructions.

Example A. NCU to CIE Block Transfer

```
        DEV1 = 0.                   CLEAR
        B = PGIN.                   PG PGIN
        OUT1 = B.
        OUT0 = 0.                   WD 0
        DEV1 = 96.                  ACCESS NCU
        OUT1 = 0.                   PG 0
        OUT0 = 0.                   WD 0
        DEV1 = 80.                  INIT TRANSFER TO NCU
        B = 180.                    TIMING PARAMETER FOR WAIT
LP1.
        B = B+1.                    INCR B
        IF ABT SKIP ELSE STEP.      =255?
        GOTO LP1.                   NO, LOOP BACK
        DEV1 = 1.                   TERMINATE TRANSFER
```

Example B. CIE to NCU Block Transfer

Same as Example A except DEV1 = 104. rather than 80.

Example C. EXO to CIE Block Transfer

```
        DEV1 = 0.                   CLEAR
        BEX2 A2 = A2.               RESET BIT REG
        B = PGOT.                   PG PGOT
        OUT1 = B.
        OUT0 = 0.                   WD 0
        DEV1 = 2.                   INIT TRANSFER
        B = 180.                    TIMING PARAMETER
LP3.
        B = B + 1.                  INCR B
        IF ABT SKIP ELSE STEP.      = 255?
        GOTO LP3.                   NO
        DEV1 = 1.                   TERM. TRANSFER
        STEP.
        BEX2 A2 = A2.               SEND STATUS REG
```

Example D. CIE to EX0 Block Transfer

Same as Example C except use DEV2 = 1. rather than BEX2, and DEV1 = 4. rather than DEV1 = 2.

Example E. Hard Interrupt NCU

```
        DEV0 = 1.                   SOFT INT
        DEV3 = 1.                   HRD INT
*       WAIT 7 MSEC FOR NODE SYNCH (14 MSEC LOW SPEED)
        B = 248.                    TIM PAR
        A1 = B.
        A2 = 0.
INLP1.
        A2 = A2 + 1.                INCR A2
        IF ABT SKIP ELSE STEP.      = 255?
        GOTO INLP1.                 NO
        A1 = A1 + 1.                INCR A1
        IF ABT SKIP ELSE STEP.      = 255?
        GOTO INLP1.                 NO
        OUT3 AMPCR = AMPCR.         RESET EXT
        OUT3 AMPCR = AMPCR.
```

Microcode Object Files which are stored on tape may be moved to disk using the file transfer (FLX) utility with a fixed binary switch fixing 256 byte record lengths; e. g. :

```
FLX DK0:/FB:256. =MT0:[1,20]XXX. OBJ
```

SECTION 5

THEORY OF OPERATION

This section provides a brief description of the theory of operation of the ESM. It is subdivided into: 1) Functional Description, 2) Nodal Hardware Description, and 3) Nodal Software Description. Additional details regarding the hardware and the software can be found in the Hardware Maintenance Manual, and in the Software Maintenance Manual, respectively.

5.1 FUNCTIONAL DESCRIPTION

5.1.1 Introduction

The Exploratory Systems Control Model (ESM) is implemented in the form of three interconnected communication loops, each consisting of up to four nodes. Each node is made up of two parallel processing Burroughs Mini-D B 7* microprocessors. The nodes on each loop are of two types: Local (L) nodes which interface either a host computer or a terminal device to the loop, and Gateway (G) nodes which interface to a similar node in another loop to implement loop-to-loop transfers. The ESM provides for highly decentralized operation, high reliability, high survivability, modularity, ease of modification, and failsoft operation. The implemented protocols and associated nodal software (written in microcode) provide a user-transparent, distributed communications scheme in which messages, which are sent to logical destinations, are routed automatically to their correct hardware destinations. The system provides for the implementation of various control and text type messages (or packets) which may be used to modify various memory locations within the nodal software, or which may be used to indicate broadcast, acknowledgement (ACK), or negative acknowledgement (NAK) type messages. Also provided is the ability to implement automatic alternate routing for the case of an inoperative gateway node, and rapid reconfiguration for the case of added or deleted nodes.

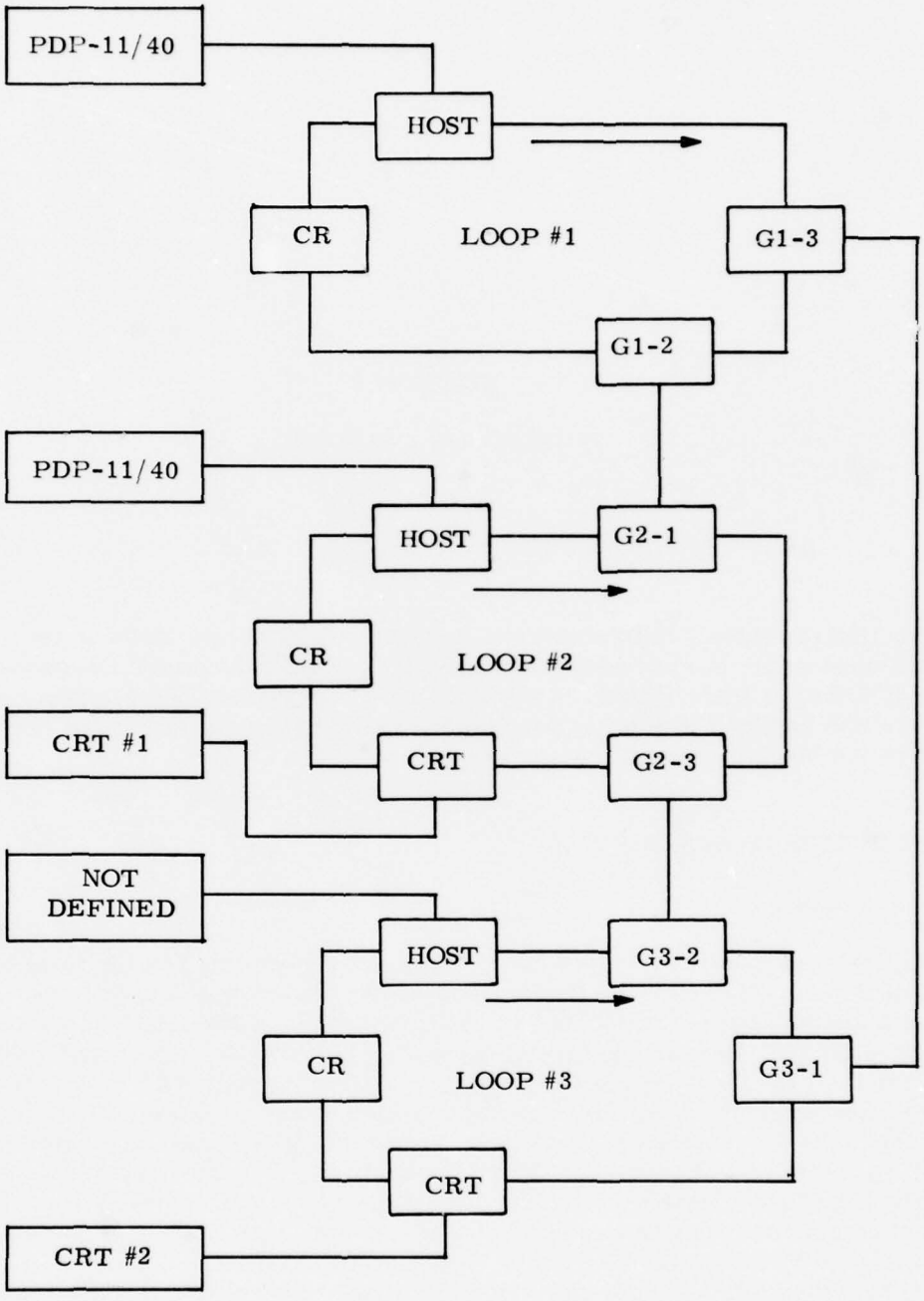


Figure 5-1. Function Configuration

The ESM loop protocol provides the foundation for extensive error detection and recovery strategies. The extent and sophistication of these error recovery schemes are limited only by the amount of programming performed either in the host computers or in the nodes. Thus, the ESM loop protocol provides a system control architecture that is relatively secure from total failure.

5.1.2 Communications Network

The communications elements that comprise the basic ESM Multiloop System are shown in Figure 5-1. There are three communications loops each having one or two local nodes and two gateway nodes. Local nodes are associated with Host computer attachment or CRT attachment to a loop, and gateway nodes are involved in loop-to-loop attachment.

All nodes are the same with each having a line interface unit (LIU) and a B7* microprocessor nodal control unit (NCU). The LIU and the NCU provides for loop interface and protocol handling. Each node includes a second B7* microprocessor which controls the node and acts as an interface for external equipment. This second microprocessor is called the Control and Interface Equipment (CIE). Each CIE is essentially the same as any other CIE except for microprogram. For L-nodes, the CIE interfaces with external equipment; for G-nodes, the CIE interfaces with another CIE of an adjacent loop. A generalized node configuration is shown in Figure 5-2.

Each node can pass data through its LIU along its loop, extract data from the loop for storage in the NCU, or take data from the NCU and inject it into the stream of data circulating in the loop. The CIE gives general directions to the NCU and may take data from, or give data to, the NCU. The NCU operating with a 1MHz or lower clock speed is synchronous with the LIU and the data stream. The CIE operates asynchronously and at a higher (8.96 MHz) clock rate.

Each loop has a Clock-Retimer (CR) which establishes the frame format for the loop and restandardizes the time slots and data elements on the loop.

5.1.3 The Data Stream

The data stream is a bit-serial set of frames. Each frame is 20T in duration and contains 20 time slots, each of which is T in duration. Each 20T frame is divided into two fields, an address field followed by an information field, each 10T in duration. T is selectable in one of three values as determined by the card mounted switches. Values of T available are 1.04 μs, 3.57 μs and 83.3 μs. These correspond to loop rates (including overhead bits) of 960 KBps, 280 KBps and 12 KBps, respectively. Actual information rates are somewhat lower as indicated later.

The first two time slots of each field provide synchronization and identify the type of field; the last eight provide a byte of information called the address word and the information word, respectively.

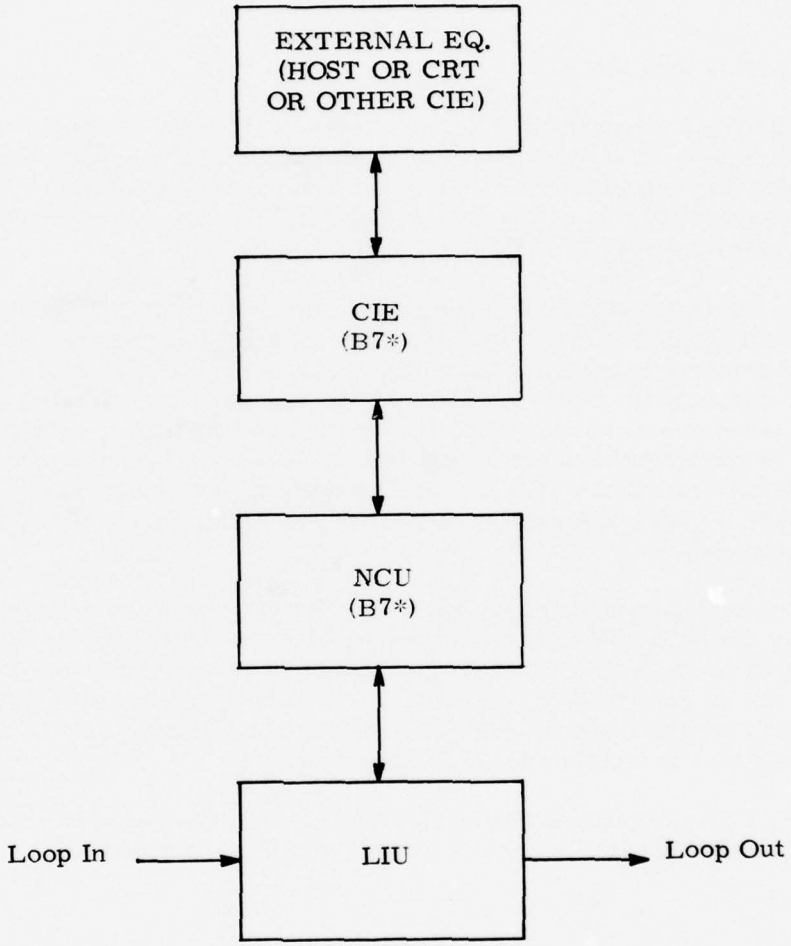


Figure 5-2. Generalized Node Configuration

Typical address and information fields are shown in Figure 5-3. A transition occurs at each T start to provide clocks except at the synchronization points (shown as a dot at the 1T point in Figure 5-3a and at the 11 T point in Figure 5-3b). A mark (high level) after the dot means Address (A in Figure 5-3a); a space (low level) after the dot means Information (I in Figure 5-3b). In the address and information words that follow A and I, transitions always occur each T. A mark after each transition, in the second half of each time period T, means One; a space means Zero. The maximum frame rate, therefore, is 50,000 per second based on a T of 1 μs. The node can write only once in two frames because of a delay caused by address and data insertion. Therefore, the effective loop capacity is 25,000 characters per second for a T of 1 μs. For the actual T's provided by the ESM, the following are the effective loop capacities:

T	Loop Capacity	Loop Rate	Information Rate
1.04 μs	24,000 ch/s	960 KBps	192 KBps
3.57 μs	7,000 ch/s	280 KBps	56 KBps
83.3 μs	300 ch/s	12 KBps	2400 Bps

A node has three modes of operation, namely: repeat, read and write. The repeat mode involves no NCU control. In this mode the node supplies a 10T delay and reforms the pulses so that the node acts as a delay repeater.

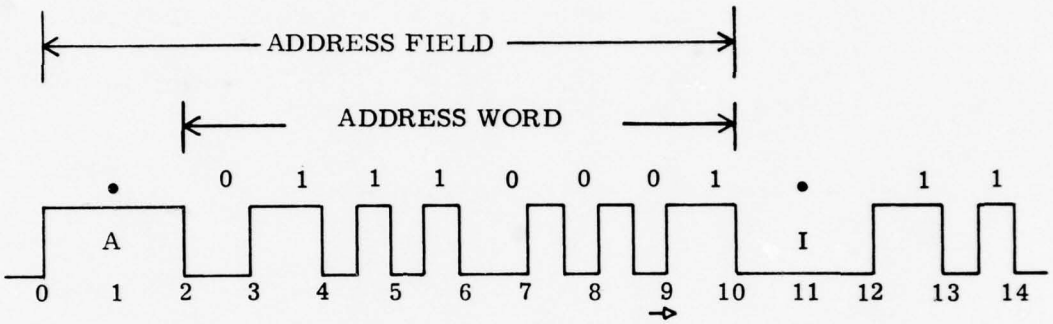
When the NCU desires to read, it sets an 8-bit address in the LIU address register and places the LIU in Read mode. The NCU then inhibits its own clock and thereby shuts off.

The LIU senses address fields in the data stream. When an address word does not match the node address, the node acts as a delay repeater. When an address word matches the node address the LIU sets the address word to zero and removes the clock inhibit of the NCU so that the NCU starts at the proper time for the data word to be read into its external input register.

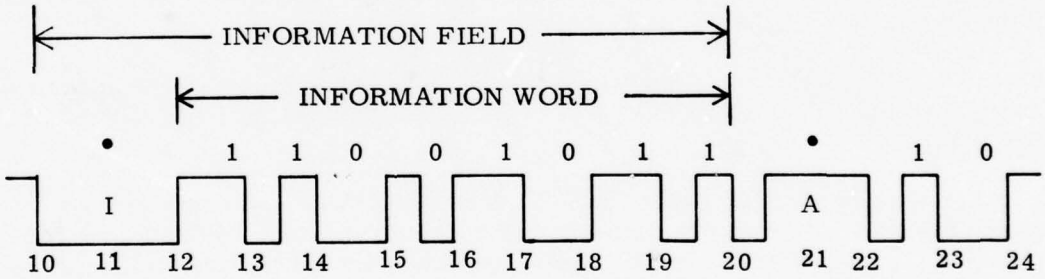
When the NCU desires to write, it sets the 8-bit address register of the LIU and places the LIU in the Write mode. The NCU then inhibits its own clock and shuts itself off.

The LIU removes the clock inhibit of the NCU so that the NCU starts at the proper time to output its address into the address frame of the data stream of the loop and to output the content of an output register into the information frame of the data stream of the loop. When the Write is complete a new address may be placed in the address register of the LIU. The NCU then enters the Read mode.

The CIE processor controls the NCU by instructing it to go into a Read or a Write mode and thus controls data transfer between itself and the NCU.



Time in Time Units T
(a) Address Field



Time in Time Units T
(b) Information Field

Figure 5-3. Address and Information Field Formats

5.1.4 Packet Description

A packet is a sequence of alternating address and information fields consisting of, at most, 256 frames. A message consists of an ordered set of packets.

The ESM loop protocol is implemented by protocol type information words which are written into the beginning and end information words (i.e., header and trailer) of a packet. These protocol type information words, which will be referred to as "protocol characters", are actually data patterns which are interpreted by the node, and are not to be confused with the address words which make up the address fields that precede every information field. The existing protocol characters and their location within a packet are given in Table 5-1.

Table 5-1. ESM Protocol Characters

D1	Packet Sequence Number
D2	Message Sequence Number
D3	Control Character
D4	Broadcast Character
D5	Destination Logical ID
D6	Source Logical ID
D7 ⋮ DN-2	Packet Information which is ignored by node and is destined for host or another CIE
DN-1	End-of-Packet Character (EOP)
DN	Longitudinal Parity Check (LPC).

In Table 5-1, N is the overall packet length equal to, at most, 256 characters. Characters D1 - D6, DN-1 and DN are the protocol characters and D7 to DN-2 are the packet information characters. The packet information characters may use any desired code such as ASCII, EBCDIC, etc.

D5 can handle 256 unique logical ID's. Several of these, however, are reserved. The value 255 is reserved for the "write token" or free packet which will be described later. A few will be reserved for special control purposes such as Broadcast. The value zero should not be used because it represents the null value. The same remarks apply to D6. D3 is for control purposes as shown in Figure 5-4.

D4 is used only for Broadcast messages wherein a proper Broadcast D5 is used and D3 has the value 1 in the seventh bit position. During Broadcast, D4 is marked by certain nodes to ensure that each node receives the message once and only once. Broadcast mode will be explained in detail later.

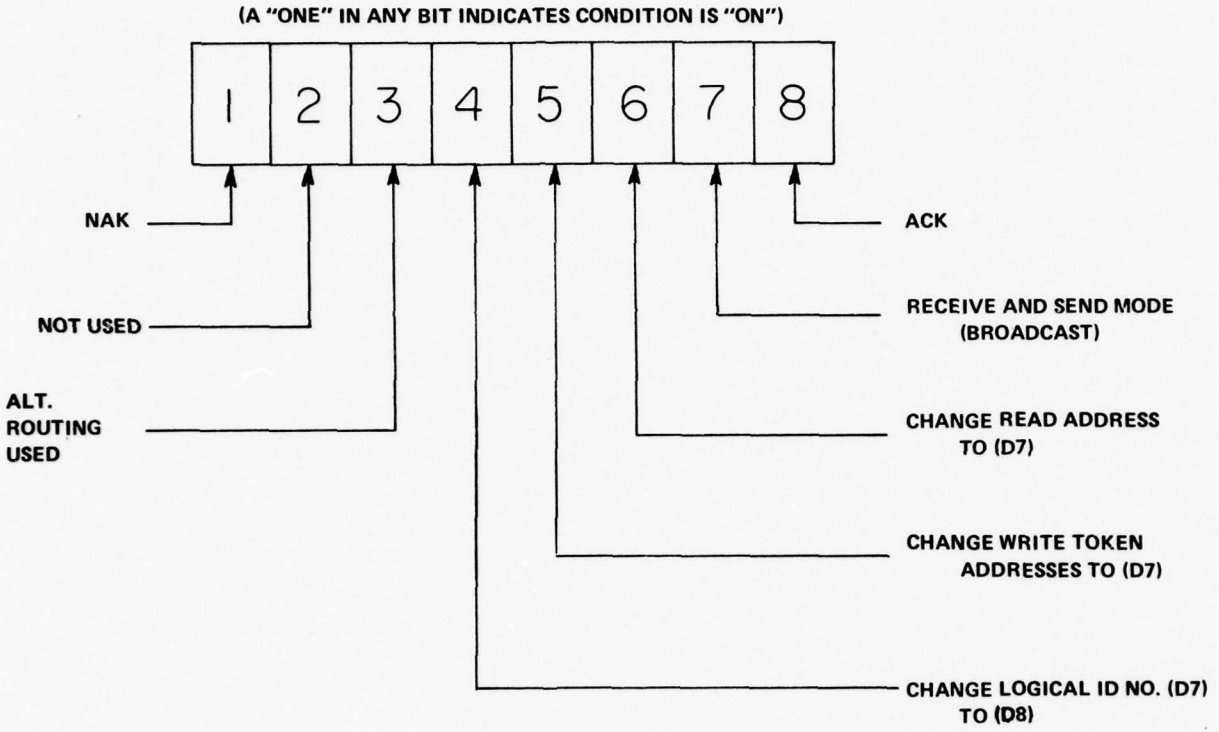


Figure 5-4. Control Word Bit Identification

D1 assures the assembly of packets into a message through the use of consecutive packet numbers within a message. Similarly, D2 provides a message sequence number to allow for separation of messages from a given logical ID.

The control word D3 provides for the implementation of control packets corresponding to functions defined in Figure 5-4. Since they may consist of only a small number of control-oriented characters, these control packets represent only a small overhead in loop traffic. For example, a NAK or ACK type control packet consists of only eight characters:

ACK or NAK packet $\triangleq$
- D1 - Packet sequence number
- D2 - Message sequence number
- D3 - Control ACK or NAK
- D4 - Broadcast = 0
- D5 - Dest. logical ID
- D6 - Source logical ID
- D7 - EOP
- D8 - LPC

Another very short control packet is the write token (WT) that consists of only two characters:

WT $\triangleq$
- D1 - EOP
- D2 - LPC.

A valid WT LPC will equal the address word to detect the occurrence of erroneous WT's generated by noise on the loop.

The write token is used to achieve a rapid type of implicit polling which will be described below. DN-1 is the end-of-packet word which is equal to eight consecutive "ones". This bit pattern was chosen because it is a unique word that does not exist as a transmitted character in any of the usual transmission codes and because it is an existing Mini-D condition test (i. e., the all bits true test, ABT) which is used to implement variable length packet sizes for ESM. The final information word is used for a longitudinal parity check which is an XOR operation performed on every information word of the packet, and it is used to determine whether an ACK or NAK type response should be sent to the packet originator.

5. 1. 5 Address Directed Protocol

An address directed protocol was found to provide an attractive foundation for implementing ESM in a rapid, efficient, and reliable manner. Each node on a loop will have a register set to a unique read or functional address within the loop; each node will have the ability to sense address fields, ignoring those fields that are not equal to its read address, and reading into its memory the information

word following an address field that is equal to its read address. A node will have permission to write a packet onto the loop only when it has received the write token (WT) which has a logical ID equal to 255, i. e., an all ONEs bit pattern. The WT will be sent from node to node around the loop. That is, a node reads the WT addressed to it, writes a packet if it has anything to write, and then sends the WT on to the next node in the loop. The orbiting WT defines an implicit polling scheme which allows a group of M nodes on a loop to write information directly to a destination without interfering with each other. This implicit polling scheme is much faster than an explicit polling scheme in which handshaking messages are passed back and forth causing a large overhead setup time. If worst-case conditions are assumed (in which everyone on the loop desires to send a packet at once) the time it takes for a write token to travel completely around the loop or the maximum time a node must wait before another packet can be written is given by:

$$T_{WT} = \frac{MP}{C_L} \qquad (1)$$

where M is the number of nodes on the loop, P is the maximum packet size given in characters, and C_L is the loop capacity given in characters/sec. Considering that the average WT cycle time will be less than the maximum obtained, assuming worst case conditions, the WT cycle time will be between the limits,

$$\frac{MK}{C_L} \leq T_{WT} \leq \frac{MP}{C_L} \qquad (2)$$

where K is the number of characters comprising a WT adjusted to reflect any processing time that the node takes to recognize that it has received a WT.

For the case of ESM, if we assume that M = 4, P = 256 characters, and C_L = 24,000 characters/second, then under worst-case conditions, the WT cycle time will equal approximately 43 milliseconds.

Since the worst-case WT orbit time for a loop is known, nodal software may provide for the creation of a new WT if one is not received within MP/C_L seconds. Furthermore, each node that has the WT has the ability to destructively write onto any address and information field thus erasing any invalid characters that may circulate the loop due to bit inversions or packets sent to down nodes. Thus, the protocol guarantees that the loop can never become clogged due to unreceived packets or a lost WT.

The address directed protocol provides near instantaneous communication between two nodes on a loop. Since intermediate nodes ignore packets that do not have address fields corresponding to their read addresses, a direct line connection is made between a node possessing the WT and its destination node on the same loop.

The nodes also provide for a delay when a packet is destined to the same node as the WT. ACK and NAK type packets are sent before a regular packet transmission.

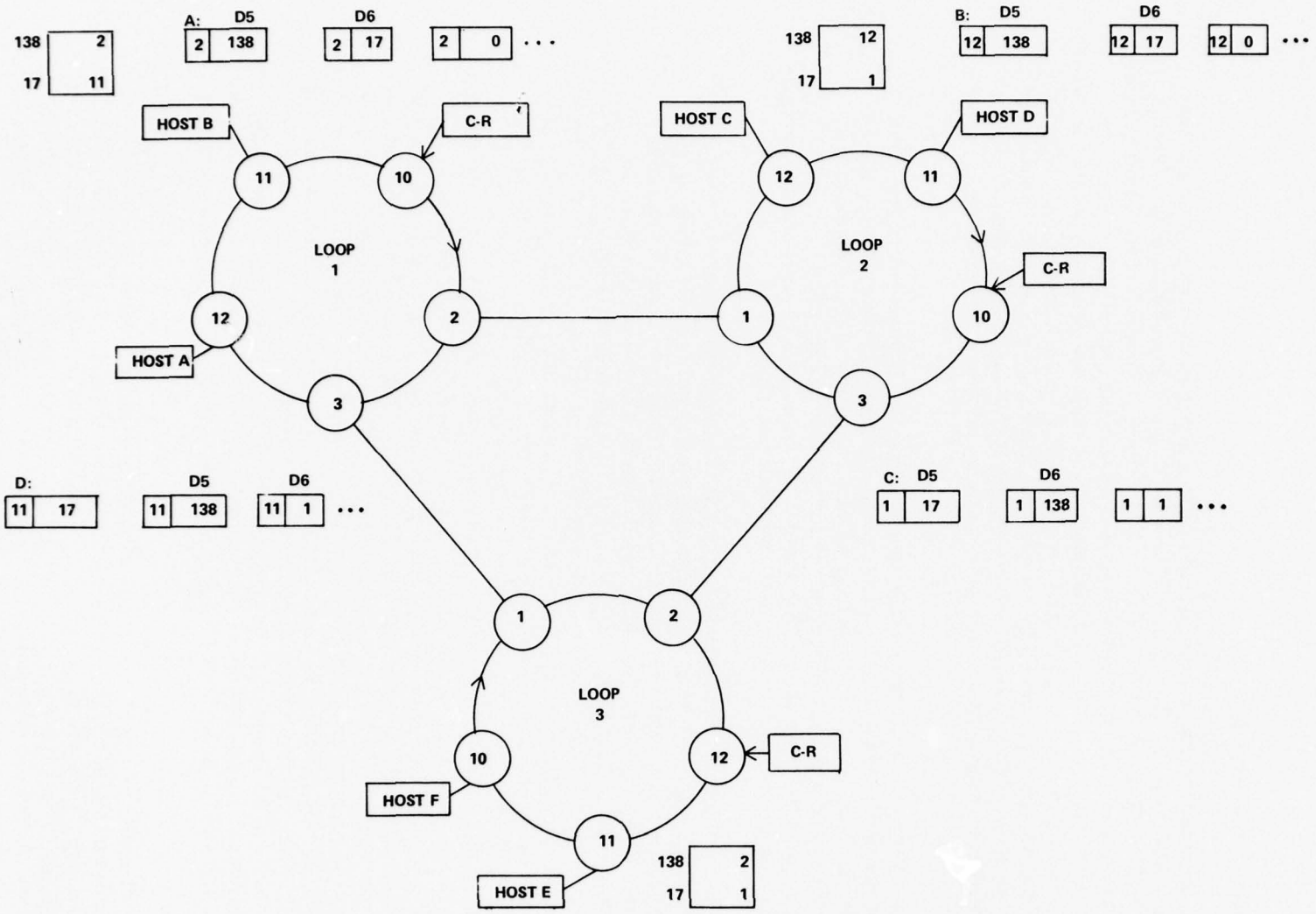
5.1.6 Method of Addressing

The address directed protocol is implemented in the nodes by means of a simple table look-up. The table is stored in a 256-word page in each nodal data memory, and it maps logical ID's to nodal functional addresses. For each data memory location on the conversion page corresponding to a particular logical ID, there is an 8-bit representation of the functional address of the node associated with that logical ID. A node wishing to send a message to logical ID of value X sends each information word of the message preceded by an address word having the value contained in location X of the node's conversion table page. Rapid reconfiguration of the network is possible using this scheme merely by modifying this page in each node's memory.

An example of this method of addressing is illustrated in Figure 5-5. The read addresses of the nodes are given for each node. Note that gateway node read addresses equal the loop number of the loop to which they interface. Suppose that host B wishes to send a packet to logical ID 138 which resides on host C. Host B uses its own logical ID 17 as the source logical ID which will be used as the destination logical ID for the return ACK or NAK type packet.

Host B supplies the information words to the CIE which determines the functional write address for logical ID 138, and it sends a packet onto the loop having the form of packet A when it receives a WT. Gateway Node 2 on Loop 1 reads the packet destined to it and sends the information words across the interface to Loop 2. Gateway Node 1 of Loop 2 then looks in its conversion table and sends packet B onto the loop. Node 12 of Loop 2 reads the packet and determines whether the LPC character checks or not. If we assume the LPC does check, the CIE delivers information words to Host C and sends an ACK type packet having the form of packet C to logical ID 17. The packet is read by Gateway Node 1 of Loop 2 which transfers the information words to Gateway Node 2 of Loop 1. Finally packet D is sent on Loop 1 which is read by Node 11 which pairs the ACK to a packet on its outstanding packet list. Note that if the connection between Loop 1 and Loop 2 was inoperable, alternate routing could be used if the CIE connected to Host B sent its packet to Gateway Node 3 of Loop 1 and set D3 = 32 to indicate alternate routing. The packet,would thus reach Loop 2 via the Gateway nodes of Loop 3. An originating node can determine whether or not a packet ever reached its destination by waiting for an ACK or NAK within a certain predetermined amount of time. If a NAK is received or there is no response, the originating node may try again to send the packet,possibly by an alternate route. Alternate routing is implemented merely by changing the address words to the functional address of the other gateway node on the loop.

The address directed protocol possesses attractive features which provides a simple implementation of certain kinds of control messages. For example, various types of broadcast messages may be implemented by assigning a special broadcast logical ID and modifying the control information word (D3) so that the message is placed in the receive and send mode (c. f. Figure 5-4). A node which receives a message that is in the receive and send mode will retransmit the message to the



Note: This figure illustrates the addressing technique only and does not specifically depict the exact ESM loop configuration.

Figure 5-5. Method of Addressing

functional address that is specified in its logical ID to functional address conversion page in the location given by the special logical ID located in information word D5 (c. f. Table 5-1). Different types of broadcasts may be implemented using this scheme, e. g., network broadcasts, local loop broadcasts, selected host only broadcasts, etc. In a broadcast type packet, information word D4 is used to guarantee that nodes do not receive a message twice and that broadcasts are correctly quenched. The originator of a broadcast will write its functional address in D4 and then quench the broadcast when the packet travels completely around its loop at which time the originator node will recognize its functional address in D4 and not resend the packet. Whenever broadcasts travel from loop to loop via a gateway node, the left-most bit of D4 will be set by that gateway node to indicate to other gateway nodes on the receiving loop not to send the packet across the interface so that nodes do not receive a packet more than once. A gateway node that acts as the originator of a broadcast for its loop will place its functional address in D4 as well as setting the left-most bit and will then quench the broadcast for its loop when a complete circuit of the loop has occurred.

A broadcast type packet may also be used in conjunction with a special node interpreted control message (e. g., modification of logical ID to functional address page, c. f. Figure 5-4) to implement rapid network reconfigurations or for creating, destroying and moving logical ID's.

5. 2 NODAL HARDWARE

The nodal hardware (illustrated in Figure 5-6) is configured around two Burroughs B 7* microprocessors and, hence, can be described in terms of two processor-centered segments. The first segment consists of the Nodal Control Unit (NCU) microprocessor and its associated control memory, data memory, ancillary logic and loop interface logic. The primary purpose of this segment is to insert packets into the loop and to remove packets (containing an appropriate address) from the loop. Hence, it provides only for control and buffering relative to the communications loop.

The second segment consists of the CIE (Control and Interface Equipment) microprocessor and its associated control memory, data memory, ancillary logic, and external interface logic. This segment provides for overall node control, packet and message handling, traffic control and external device interfacing.

In addition to the nodal hardware of Figure 5-6 a Clock Generator, a Clock-Retimer and Loading Logic are required for each loop. The specific functions and characteristics of these units and of the individual elements of the NCU and CIE segments are described in detail in the following paragraphs.

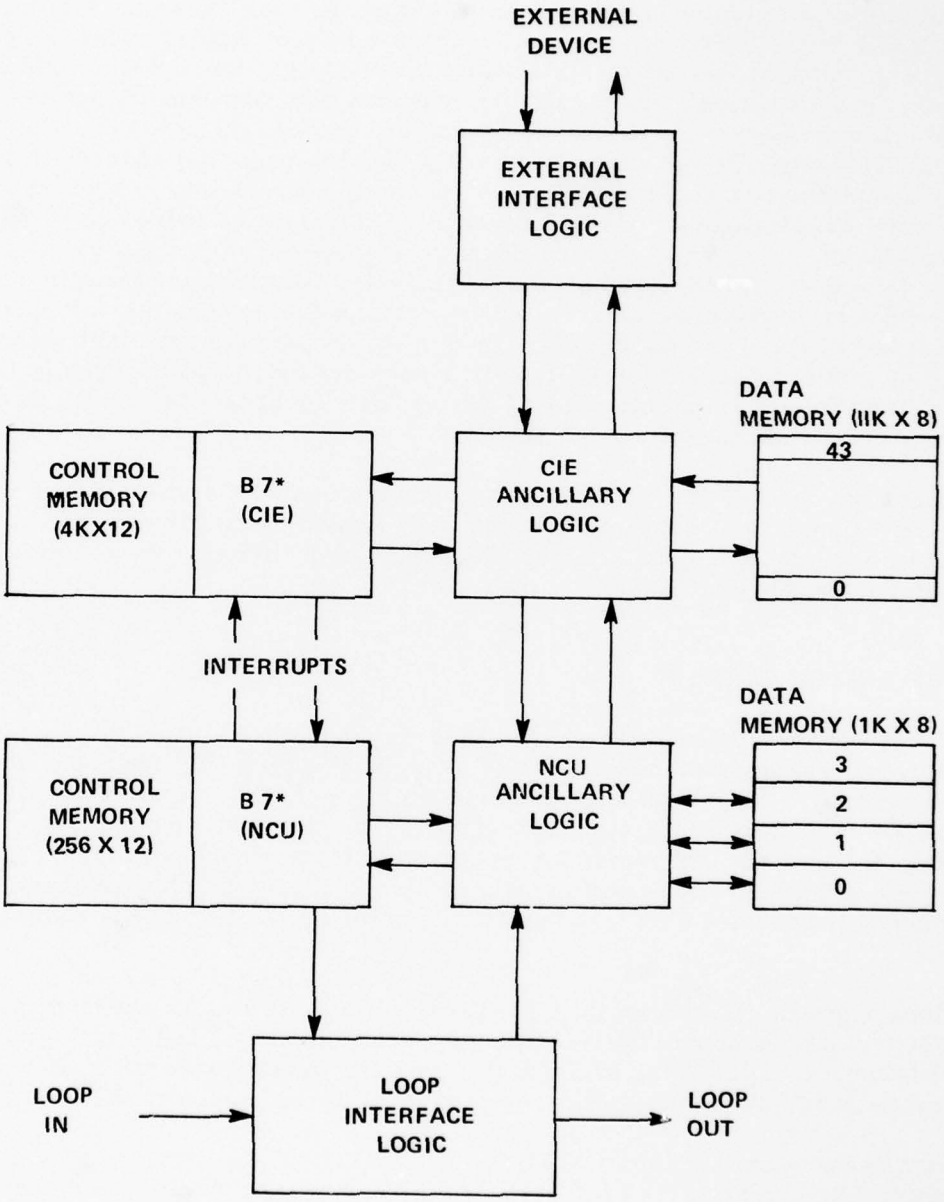


Figure 5-6. Node Configuration

5.2.1 NCU Segment

The Loop Interface element contains the necessary cable drivers and receivers for direct loop interface. It includes the circuitry for deriving clock from the data stream and for maintaining frame synchronization relative to the data stream. It contains an address register, loaded by the B 7*, and associated comparaison circuitry to permit recognition of a specific address in an address field on the loop. Upon address recognition, the information word is streamed directly into the NCU data memory, while being monitored by the B 7* for an end-of-packet (EOP) character.

The Loop Interface logic operates from one of three selectable clock rates: (1) 960 kHz, (2) 280 kHz, and (3) 12 kHz. The logic is contained on a single printed circuit board (PCB).

The NCU Microprocessor provides for control of the Loop Interface logic and the NCU Data Memory. That is, it establishes the Read or Write mode of operation (relative to the loop), sets the Loop Interface address register for a Read operation or initiates output for a Write operation, controls addressing of the Data Memory input and output locations and monitors the input/output stream for the EOP character. It interrupts the CIE microprocessor upon completion of the write/read cycle and responds to an interrupt from the CIE microprocessor to begin its next write/read cycle.

The NCU Microprocessor operates from the clock derived by the Loop Interface logic; hence, it operates in synchronism with the loop bit stream. Processor operation is bit-serial with 10 clocks (10.4 μsec) per instruction or per input/output byte (8 bits). The NCU microprocessor has 8-bit data registers, a 12-bit instruction register, and employs 8-bit memory addressing thereby permitting up to 256 words of control memory. This memory has 12-bit words and is provided in PROM form. The NCU microprocessor together with its control memory is contained on two PCB's.

The NCU Data Memory functions as I/O buffering relative to the loop and, in addition, provides a mailbox page for communication with the CIE microprocessor and for storing other loop control information. This RAM consists of 4 pages, each accommodating 256 8-bit words. It employs n-MOS semiconductor technology with a 350-nanosecond read or write cycle. It occupies one PCB.

The NCU Ancillary Logic provides for memory addressing and read/write control of the NCU Data Memory. That is, it provides NCU data memory access and control by both the NCU microprocessor and (when used with the CIE Ancillary Logic) the CIE microprocessor. It provides for serial/parallel data conversion to permit data transfer among the B 7* (serial), Data Memory (parallel) and the communications loop (serial). It permits the routing of data to/from the microprocessor and several destinations (e.g., Data Memory or Loop Interface Logic). Finally, it permits direct memory-to-memory transfers between NCU and CIE Data Memories without processor handling, but under processor initiation. The NCU Ancillary Logic is contained on one PCB.

5.2.2 CIE Segment

The CIE Microprocessor provides for control of the entire node. It communicates with the NCU Microprocessor via interrupts and via the mailbox page of the NCU data memory. In this manner, it initiates NCU microprocessor operations relating to loop interfacing and it accesses NCU data memory I/O pages to transfer data between those pages and the I/O queues of its own data memory. As mentioned earlier, these inter-memory transfers are accomplished directly (memory-to-memory) in a parallel transfer mode. The CIE B 7* determines message type (e.g., single address, multi-address, acknowledgement, etc.), does parity checking, generates ACK/NAK messages, determines alternate routing, controls I/O queues, does message assembly, loads/unloads buffers of the External Interface Logic, and maintains status of these buffers.

The CIE Microprocessor is very similar to the NCU microprocessor except that it operates from a 8.96 MHz clock with 9 clocks per instruction and employs 12-bit memory addressing, thereby permitting up to 4K words of control memory. This memory has 12-bit words and is in the form of external RAM on two PCB's. The CIE microprocessor (like the B 7* NCU) is contained on two PCB's.

The CIE Data Memory primarily provides storage for assembling and queueing messages (in the form of packets) to/from the communications loop as well as to/from the external device. It also provides for storing user address and routing information, and includes work page capability. This RAM consists of 44 pages each accommodating 256 eight-bit words (i.e., a total of 11K words). It employs n-MOS semiconductor technology with a 350-nanosecond read or write cycle. It is contained on three PCB's.

The CIE Ancillary Logic provides for memory addressing and read/write control of the CIE Data Memory; together with the NCU Ancillary Logic it provides for access and control of the NCU Data Memory by the CIE Microprocessor. It also provides serial/parallel data conversion to permit data transfer among the CIE B 7* (serial), Data Memory (parallel) and the External Interface Logic (parallel). It permits the routing of data to/from the microprocessor and several destinations (e.g., data memory, memory address register, interface logic, etc.). Finally, it permits direct memory-to-memory transfers between CIE and NCU data memories without processor handling, but under processor initiation. The CIE Ancillary Logic is contained on one PCB.

The External Interface Logic permits interface with an external host computer, an external CRT terminal, or another communications loop. It provides the necessary I/O buffers and controls to allow data transfer to/from the I/O queues of the CIE Data Memory and the external device (host computer, CRT terminal or communications loop). Data is transferred between data memory and the I/O buffers in the direct parallel transfer mode without processor handling, but upon processor initiation. Buffer status registers are set by the buffers and are read by the processor. Flags are set by the buffer and by the external device to control external data transfers in serial form. Necessary line drivers are included in the External Interface Logic.

This logic is contained on one PCB for each type of external device.

5.2.3 Clock Generator

The clock generator develops the various clock signals required for the proper operation of the loop and its interconnected nodes. It consists of two separate crystal oscillators and the associated divider and driver logic to derive and output the necessary clock signals. The primary clock signals developed and their uses are:

Clock Signal	Function
8.96 MHz	CIE clock
1.92 MHz 560 KHz 24 KHz	NCU and Loop clock (one rate per loop, selected by card-mounted switches, and divided by two by CR)
560 KHz	Host Interface clock and Gateway Interface Clock
96 KHz 9600 Hz	CRT Interface clock
96 KHz 2.8 KHz 1.2 KHz	Real time clock for CIE (one rate per loop selected by card-mounted switches).

Other logic clocks are also generated and distributed to the PCB's of each node.

5.2.4 Clock-Retimer

A clock-retimer is provided for each communications loop. It accepts the loop clock signal from the clock generator and establishes the previously described loop frame format. It also accepts the data signal from the loop and provides data regeneration and data resynchronization, thereby compensating for effects relative to signal degradation and propagation time. This logic is contaired on one PCB.

5.2.5 Loading Logic

The Loader Board and the Loader ancillary board together provide the capability to load the CIE control memories of each of the ESM nodes. These boards accept serial data (and associated clock) from the Host PDP-11/40 that is connected to ESM Loop #2. This data, at 560 KBps, is routed to the appropriate control memory as a result of proper setting of the panel-mounted switches (on each cabinet) that are used for loading.

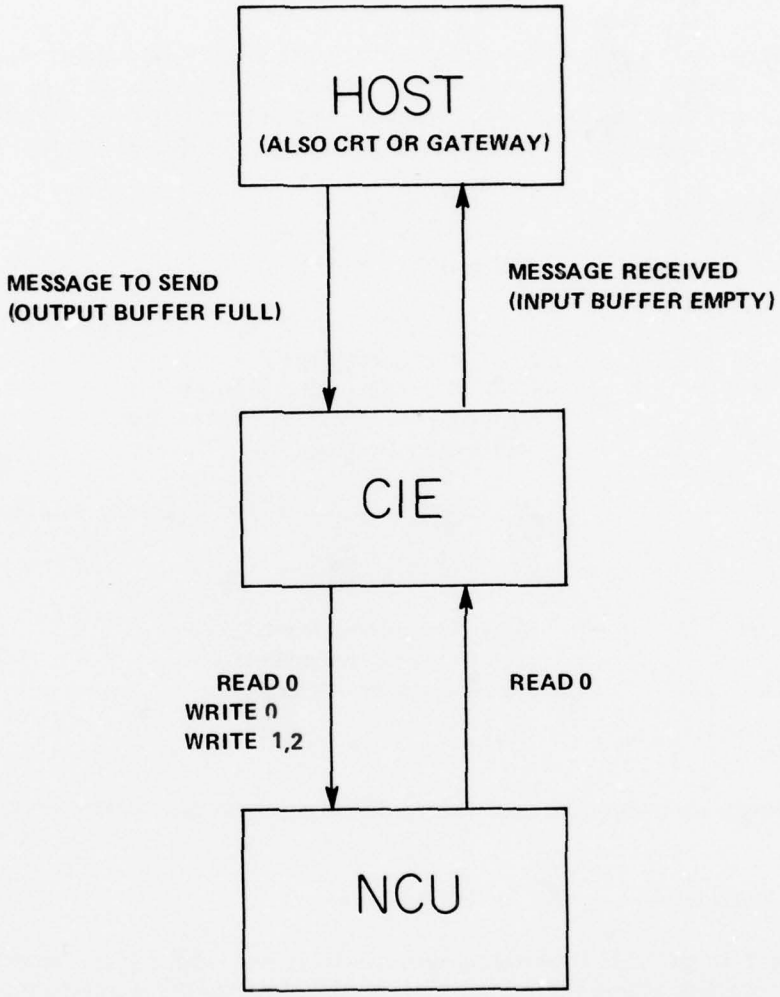


Figure 5-7. System Data Flow

5.3 NODAL SOFTWARE

5.3.1 Data Flow

This section summarizes the nodal software required to implement the address-directed protocol for the ESM. A node consists of two Burroughs B7* Microprocessors operating in parallel. One of the microprocessors, the Nodal Control Unit (NCU), is used to read and write information onto the loop via a line interface unit (LIU). The second processor, the Control and Interface Equipment (CIE), is responsible for intelligent control of the node, and acts as an interface for external equipment which may be a host computer, a CRT terminal or another CIE. The NCU has an associated 256 twelve-bit word control memory, and the CIE has an associated 4K words of control memory. The CIE has access to a data memory consisting of 12K words (bytes or characters of eight bits). The NCU has access to 1K of this same data memory.

The B 7* machines are programmed in microcode (i.e., MDMPL). The CIE microprocessor is able to handle data from both the NCU and host computer or CRT or gateway. The NCU may interrupt the CIE and vice-versa via the B 7*'s External (EXT) control line which may be tested by an IF EXT type condition test instruction. The type and source of data is communicated to the CIE by means of external registers to which the originating processor has access. The nodal software was developed using a top-down modular approach that conforms to structured programming techniques.

The system data flow is illustrated in Figure 5-7. The NCU interrupts the CIE after it has read a packet. The host computer (or another Gateway CIE) informs the CIE when it has a message to send. The CIE interrupts the NCU and instructs it either to go into the Read state to read a packet addressed to it, or to go into the Write state to write a broadcast type packet onto the loop or to write a singly addressed output packet onto the loop. The CIE interrupts the host whenever it receives a message destined for the host.

The interrupts labeled "read" or "write" between the NCU and CIE are shown with numerals "0", "1", or "2." These numerals refer to page addresses in data memory that are shared by the NCU and CIE. The functions assigned to these pages are explained below.

5.3.2 NCU - CIE Shared Memory

The total nodal data memory consists of 12K 8-bit words divided into 48 pages of 256 words each. The first four pages are addressable by both the NCU and the CIE, but disjointly in time. When the NCU operates as a nodal controller, the shared memory is the NCU memory; when the NCU is waiting for an EXT interrupt, the CIE may control the shared memory.

These four pages are shown in Figure 5-8 and are labelled as pages 0, 1, 2 and 3. Page 0 is used as an input buffer for packets received by the node. Page 2 is the output buffer for packets to be sent by the node. Page 1 is the mailbox. Page 3 is not

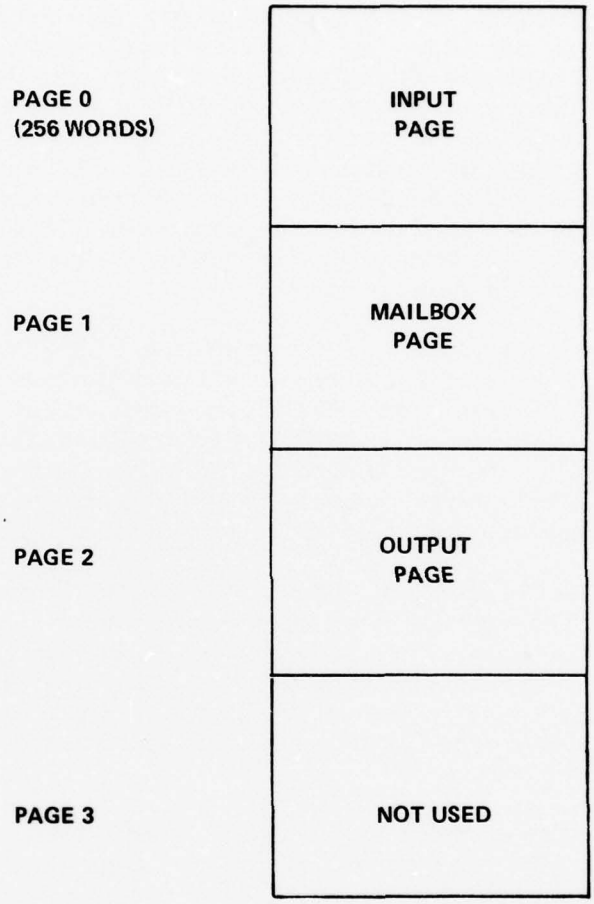


Figure 5-8. Common NCU-CIE Access Pages in Data Memory

currently used. Page 0 may also be used as a read-write buffer for packets that are received by the node in a receive/send mode of operation such as that used for broadcast type packets.

Page 1 (the mailbox) has multiple uses. It stores interrupt information to be used by the NCU, it stores parameters such as the node's read address, and ACK-NAK messages which are to be written to the loop upon receipt of the write token (WT). Figure 5-9 shows the content of the mailbox.

When a WT is received, the ACK-NAK packets are sent followed by the content of the output page. The WT is then sent to the next hardware address which is obtained from page 1.

The remaining 44 pages of data memory are accessed only by the CIE. Page 0 of the CIE memory is a workpage which is used to store commonly used variables, queue status indicators, and scratch-pad areas for storing temporary variables. Page 1 is used as the logical-ID to functional address page which is illustrated in Figure 5-10. This page is used to translate rapidly a logical ID to a write or functional address. The write address is then used by the NCU to set its address register to generate the proper address words. The other pages in data memory are used for storing packets in the input to host queue and the output to loop queue. The maximum size of these queues will be determined by variables stored on the work page. The queues are described by four variables; two of which are used as pointers to the page at which the packet on the top of queue is located and the first free page, and the other two will be used to count the total number of packets currently in the queue and the maximum number in order to indicate queue overflow. There is space in the node to store a maximum of 41 packets. Page 2 of the CIE memory is used to build ACK/NAK packets which are moved to the mailbox page when the WT is received.

5.3.3 NCU Software Modules

The operation of the NCU may be described by the three-state diagram shown in Figure 5-11. The NCU is always in one of three states; namely: Read, Wait or Write. The state transitions and their causes follow:

1. Read-to-wait. This state transition occurs when a packet has been read into the input page of the NCU as indicated by the end-of-packet word (EOP). The NCU informs the CIE of this condition by setting the EXT of the CIE. The NCU then suspends operation by waiting for its EXT to be set. The read-to-wait transition is unconditional.

2. Wait-to-read. The CIE determines the type of packet in the input page. If the packet is neither a WT nor a receive/send type, the CIE sets the mailbox for read and sets the EXT of the NCU. The NCU then comes out of the Wait state and goes into its Read mode.

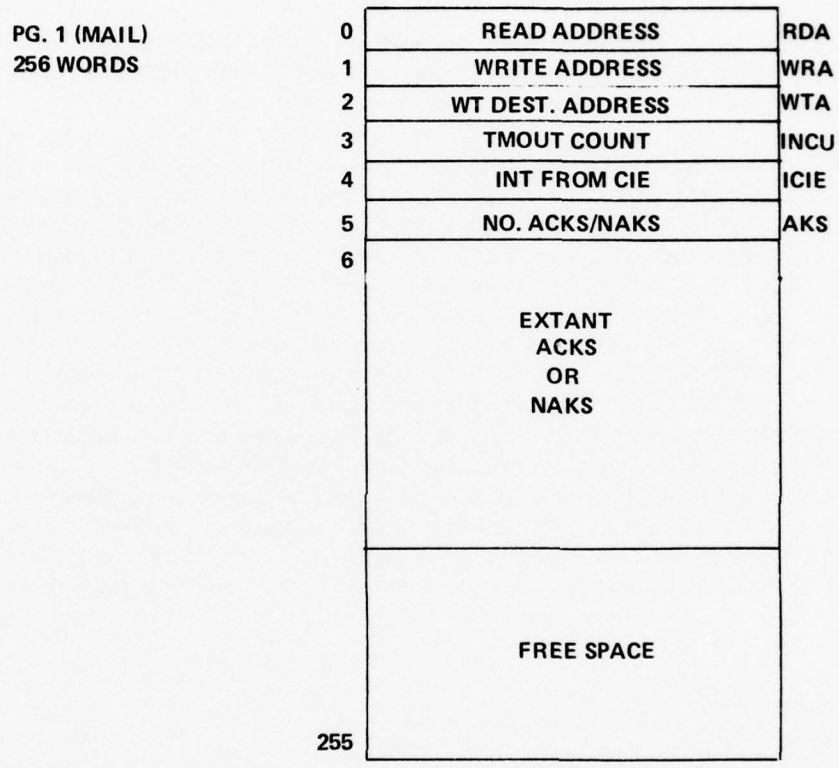
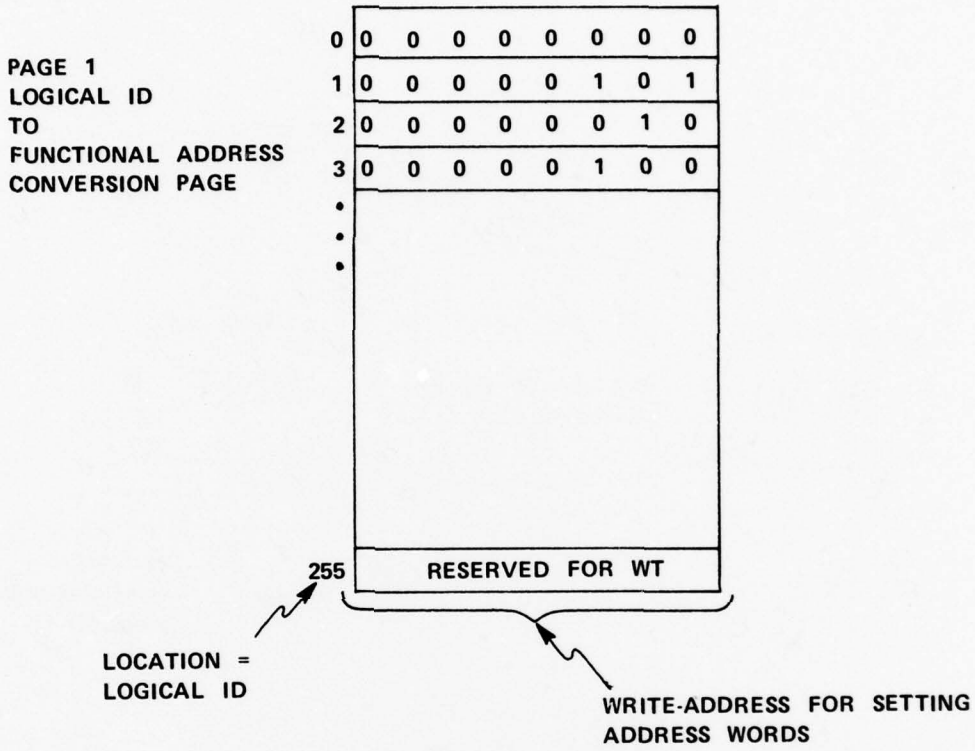


Figure 5-9. Mailbox Page Description



IF TABLE ENTRY = 0 THEN FREE LOGICAL-ID
(I.E., NOT USED IN SYSTEM)
IF TABLE ENTRY = THAT NODE'S FUNCTIONAL ADDRESS THEN LOGICAL-ID
IS PRESENT AT THAT NODE.
FOR RECEIVE/SEND MODE, TABLE ENTRY IS FUNCTIONAL ADDRESS OF
NEXT DESTINATION NODE.

Figure 5-10. Logical-ID to Functional-Address Conversion Page

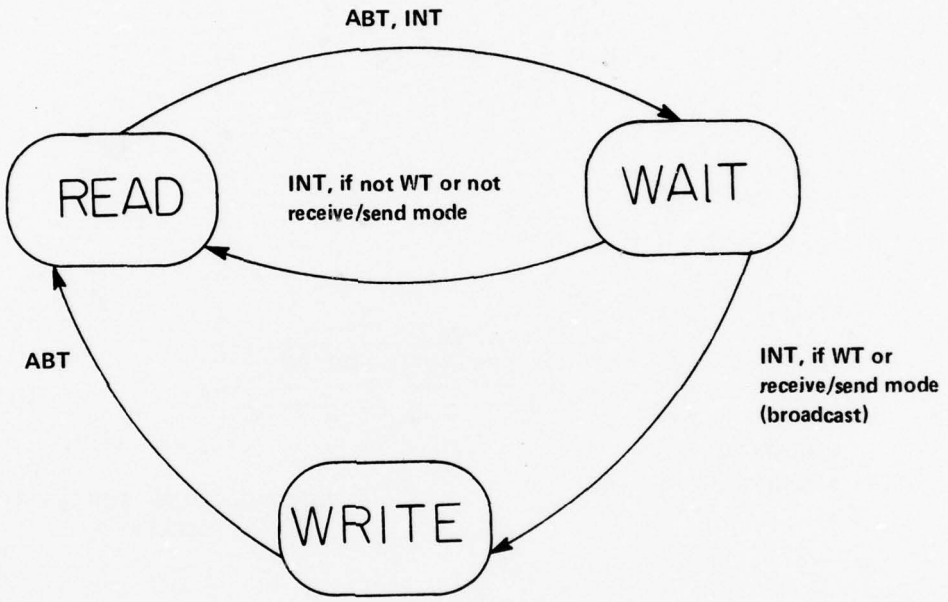


Figure 5-11. NCU State Diagram and Software Modules

3. Wait-to-write. The CIE determines the type of packet in the input page. If the packet is a WT or a receive/send type, the CIE sets the mailbox for the type of write and sets the EXT of the NCU. The NCU then comes out of the Wait state and goes into the Write state.

4. Write-to-read. This transition occurs unconditionally after write is complete.

5.3.4 NCU Software Modules

The software modules of the NCU are written to correspond to the three states; a functional description follows:

1. Read. The LIU address register is set to the read address given in the mailbox page (Figure 5-9). When the nodal logic senses an address word that is equal to the read address, the information word that follows is read into the input page and the B-register of the NCU. The data words are read into sequential locations of the input page until the EOP (all ONEs) is sensed in the B-register by an IF ABT command in the read loop of the NCU program. The information word following the EOP is also read. This is the *longitudinal parity check* (LPC) word. Exit to the read-to-wait routine is then performed wherein the EXT of the CIE is set and the Wait state is entered by a looping IF EXT instruction.

2. Wait. This module allows the CIE and NCU to acces the same data pages. The NCU dwells in this state until its EXT is set. When an interrupt does occur, the NCU examines the mailbox page to determine what type of interrupt has occurred. The possible interrupts are Read, Write 0, or Write 1, 2.

3. Write. If a Write 0 interrupt from the CIE has occurred, the NCU writes the data words of page 0 with the proper address field indicated on its mailbox page until an EOP character is found. For a Write 1, 2 interrupt, the NCU first writes any ACK type packets that may reside on page 1 and then writes the output packet residing on page 2, if any, followed by a write token sent to the next node on the loop.

5.3.5 CIE Software Modules

The CIE software that implements address-directed protocols is definable as a set of ten modules sequenced as shown in Figure 5-12. Modules on the left have higher selection priority than those on the right. This provides the quickest NCU wait-to-read transitions which must be performed rapidly to ensure that no message

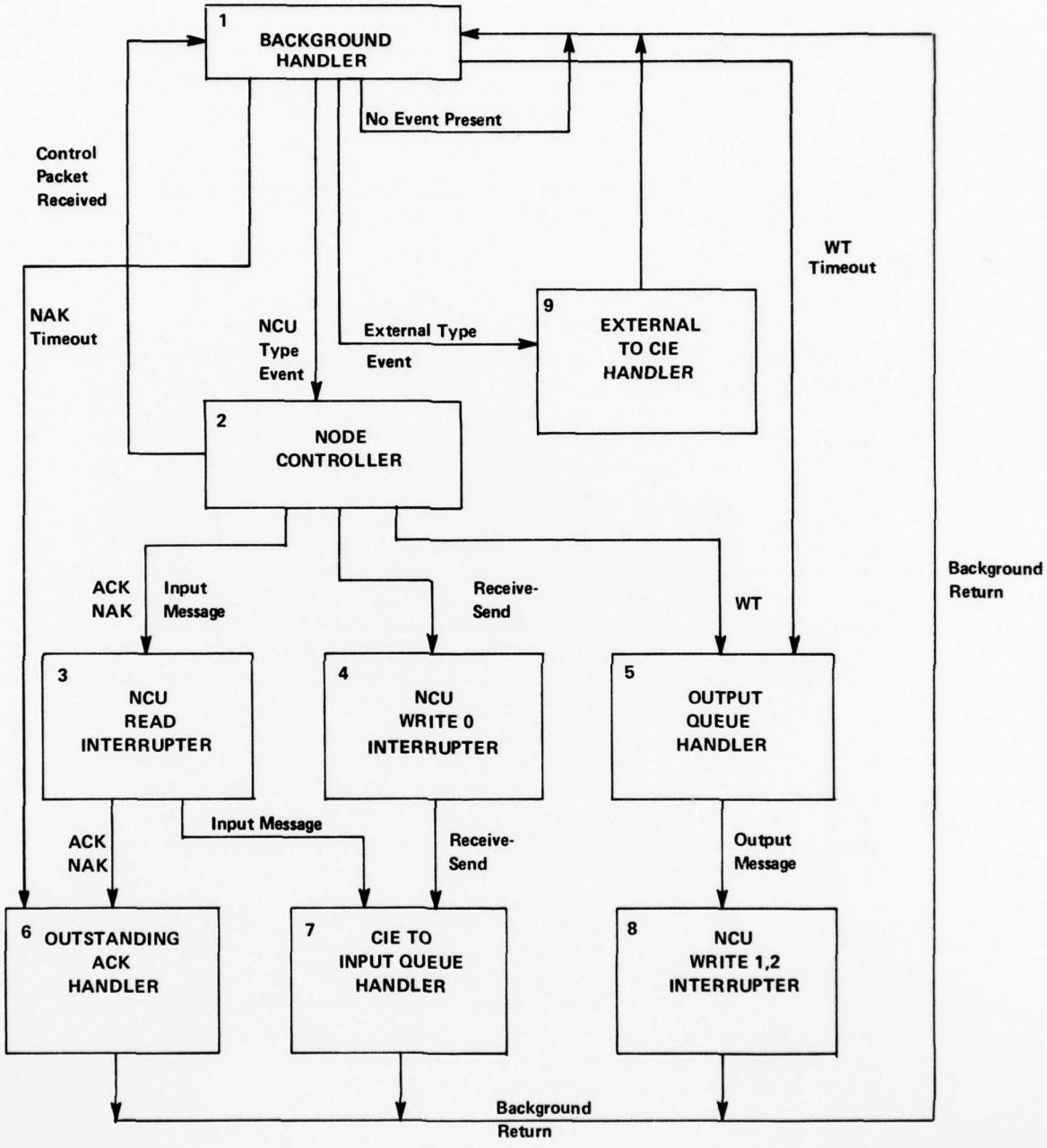


Figure 5-12. CIE Software Modules

destined for a node is missed owing to late transition to the Read state. A short functional description for each module follows.

1. Background Module. The CIE scans the events that are to be processed. If none is present, the CIE looks for an empty external input buffer (for transfer of data to external equipment – such as host or user terminal, or in the case of gateway nodes another CIE). It loads the external buffer from input queue if a packet is present. It looks for an EXT interrupt from the interface buffer. It also handles the generation of new WT's and checks packets in the output queue for retransmission timeout.

2. Node Controller. An NCU event occurs only upon completion of an NCU read-to-wait transition. The NODE CONTROLLER moves the packet on page 0 to an empty page in CIE memory. The header is then examined. For ACK, NAK or input messages the NCU READ INTERUPTER is started immediately with one exception; namely: the message is a nodal control message. In that case, one of the following is performed first.

   - Write mailbox to change hardware address;
   - Change logical-ID/functional address table;
   - Write mailbox to change WT address.

   If the input packet is of the receive/send type then the NCU WRITE 0 INTERRUPTER is started. If the input packet is a WT then the output queue handler is started.

3. NCU Read Interrupter. The read mailbox is set and the EXT of the NCU is set to cause a wait-to-read transition. For ACK/NAK inputs, the OUTSTANDING ACK HANDLER is called, otherwise the CIE TO INPUT QUEUE HANDLER is called. If the node is a gateway node, ACK/NAK inputs are treated as regular input messages destined for another loop.

4. NCU Write 0 Interrupter. The Write 0 mailbox is set and the EXT of the NCU is set to cause a wait-to-write transition. The CIE TO INPUT QUEUE HANDLER is then called. Thus a receive/send message is treated as both an input and an output message.

5. Output Queue Handler. After a WT has been received, all extant output ACK/NAK messages are moved to the mailbox. An output message (if any) is then delinked from Output Queue and moved to the NCU page 2. The NCU WRITE 1, 2 INTERRUPTER is then called.

6. Outstanding ACK Handler. An ACK received is paired to a packet previously written to the line and the packet page is marked available. A NAK received is paired to a previously written page and the page is relinked to the Output Queue for retransmission. At the end of the Outstanding ACK module, return to the Background module is performed.

7. CIE to Input Queue Handler. All input packets are handled by this module except ACK/NAK packets received at local nodes and WT packets. Input message and receive/send packets are checked for parity. If parity checks, the packet is linked to Input Queue and an ACK is added to the extant output ACK/NAK list. If parity does not check, the packet is marked null and a NAK is added to the extant ACK/NAK list. The Background module is then called.

8. NCU Write 1, 2 Interrupter. The Write 1, 2 mailbox is set. The destination for WT and the output message write address are set into the mailbox. The EXT of the NCU is then set, and the Background module is called.

9. External to CIE Handler. If an external to CIE event exists, the CIE transfers the content of the CIE buffer to the Output Queue for messages and the CIE buffer is marked empty. In gateway nodes, ACK/NAK packets may also be sent across the external interface. When received, such ACK/NAK messages are placed in the extant ACK/NAK list for transfer to the NCU at the next used Output Queue Handler. The Background module is then called.

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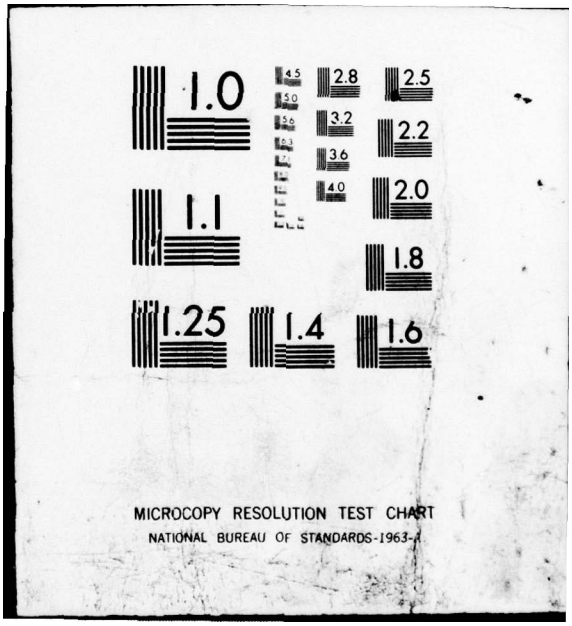
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1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

APPENDIX A

TAPE FILE DIRECTORY LISTINGS

ESM System Tapes as explained in Section 4.2 are presented here.

ESM TAPE #1 - USER LANGUAGE

```
MCR>FLX TT0:=MT0:[*,*]*.*/LI

DIRECTORY       MT0:[0,0]
18-MAR-77

RCMV1.FOR              9.     18-MAR-77 <233> [20,20]
RCMV1.OBJ             22.     18-MAR-77 <233> [20,20]
RCMV1.ODL              1.     18-MAR-77 <233> [20,20]
RCMV1.TSK             53.     18-MAR-77 <233> [20,20]
RCMV5.ODL              1.     18-MAR-77 <233> [20,20]
RCMV5.FOR              9.     18-MAR-77 <233> [20,20]
RCMV5.TSK             53.     18-MAR-77 <233> [20,20]
RCMV5.OBJ             22.     18-MAR-77 <233> [20,20]
PROC1.TSK             48.     18-MAR-77 <233> [20,20]
PROC1.OBJ             26.     18-MAR-77 <233> [20,20]
PROC1.ODL              1.     18-MAR-77 <233> [20,20]
PROC1.FOR             11.     18-MAR-77 <233> [20,20]
PROC5.OBJ             27.     18-MAR-77 <233> [20,20]
PROC5.ODL              1.     18-MAR-77 <233> [20,20]
PROC5.TSK             48.     18-MAR-77 <233> [20,20]
PROC5.FOR             11.     18-MAR-77 <233> [20,20]
M1710.FOR              1.     09-MAR-77 <233> [20,20]
M1710.OBJ              1.     09-MAR-77 <233> [20,20]
M1710.TSK              3.     09-MAR-77 <233> [1,1]
M1710.STB              1.     09-MAR-77 <233> [1,1]
INFOPM.OBJ            67.     09-MAR-77 <233> [20,20]
MSG.OBJ               36.     09-MAR-77 <233> [20,20]
EFTERD.OBJ             9.     09-MAR-77 <233> [20,20]
EFCKTD.OBJ             4.     09-MAR-77 <233> [20,20]
EFTRKD.OBJ             4.     09-MAR-77 <233> [20,20]
EFLOCF.OBJ             5.     09-MAR-77 <233> [20,20]
EFDIR.OBJ              2.     09-MAR-77 <233> [20,20]
STESM.CMD              1.     09-MAR-77 <233> [20,20]
ESMLDR.TSK            32.     09-MAR-77 <233> [20,20]
MDMPL.TSK             86.     09-MAR-77 <233> [20,20]
USROVL.ODL             1.     09-MAR-77 <233> [20,20]
P0000.OBJ             21.     09-MAR-77 <233> [20,20]
P0000.FOR             11.     09-MAR-77 <233> [20,20]
P00001.OBJ            21.     09-MAR-77 <233> [20,20]
P00001.FOR            11.     09-MAR-77 <233> [20,20]
P1000.FOR              6.     18-MAR-77 <233> [20,20]
P1000.OBJ             12.     18-MAR-77 <233> [20,20]
P10001.FOR             6.     18-MAR-77 <233> [20,20]
P10001.OBJ            12.     18-MAR-77 <233> [20,20]
P2000.FOR              5.     18-MAR-77 <233> [20,20]
P2000.OBJ             11.     18-MAR-77 <233> [20,20]
P3000.FOR             11.     18-MAR-77 <233> [20,20]
P3000.OBJ             26.     18-MAR-77 <233> [20,20]
P3001.OBJ             17.     18-MAR-77 <233> [20,20]
P3001.FOR              7.     18-MAR-77 <233> [20,20]
P4000.FOR             13.     18-MAR-77 <233> [20,20]
P4000.OBJ             29.     18-MAR-77 <233> [20,20]
P40001.FOR            13.     18-MAR-77 <233> [20,20]
P40001.OBJ            29.     18-MAR-77 <233> [20,20]
P4001.FOR             11.     18-MAR-77 <233> [20,20]
```

```
P5000.FOR                4.     18-MAR-77 <233> [20,20]
P5000.OBJ                8.     18-MAR-77 <233> [20,20]
RDLOOP.OBJ               2.     18-MAR-77 <233> [20,20]
RDLOOP.FOR               1.     18-MAR-77 <233> [20,20]
WRLOOP.FOR               1.     18-MAR-77 <233> [20,20]
WRLOOP.OBJ               2.     18-MAR-77 <233> [20,20]
HST.FOR                  4.     18-MAR-77 <233> [20,20]
HST.OBJ                 11.     18-MAR-77 <233> [20,20]
HST1.FOR                 4.     18-MAR-77 <233> [20,20]
HST1.OBJ                11.     18-MAR-77 <233> [20,20]
USRLN5.TSK              98.     18-MAR-77 <233> [20,20]
USRLN1.TSK              98.     18-MAR-77 <233> [20,20]

 TOTAL OF 1181. BLOCKS IN 65. FILES

>
```

ESM TAPE #2 - CIE MICROCODE

```
MCR>FLX TT1:=MT0:[*,*]*.*/LI

DIRECTORY       MT0:[0,0]
12-MAR-77

HST1.OBJ                9.      12-MAR-77 <233> [1,20]
GAT2.OBJ                8.      12-MAR-77 <233> [1,20]
GAT3.OBJ                8.      12-MAR-77 <233> [1,20]
CRT4.OBJ                9.      12-MAR-77 <233> [1,20]
HST5.OBJ                9.      12-MAR-77 <233> [1,20]
GAT6.OBJ                8.      12-MAR-77 <233> [1,20]
GAT7.OBJ                8.      12-MAR-77 <233> [1,20]
CRT8.OBJ                9.      12-MAR-77 <233> [1,20]
HST9.OBJ                8.      12-MAR-77 <233> [1,20]
GAT10.OBJ               8.      12-MAR-77 <233> [1,20]
GAT11.OBJ               8.      12-MAR-77 <233> [1,20]
HST1L.OBJ               9.      12-MAR-77 <233> [1,20]
CRT4L.OBJ               9.      12-MAR-77 <233> [1,20]
HST5L.OBJ               9.      12-MAR-77 <233> [1,20]
CRT8L.OBJ               9.      12-MAR-77 <233> [1,20]
CRT4S.OBJ               9.      12-MAR-77 <233> [1,20]
CRT8S.OBJ               9.      12-MAR-77 <233> [1,20]
HST9S.OBJ               8.      12-MAR-77 <233> [1,20]
CRT4.DAT              119.      12-MAR-77 <233> [1,20]
HST5.DAT              100.      12-MAR-77 <233> [1,20]
GAT7.DAT               97.      12-MAR-77 <233> [1,20]
HST9.DAT              102.      12-MAR-77 <233> [1,20]
ESMLDR.FOR              2.      12-MAR-77 <233> [20,20]
ESMLDR.OBJ              5.      12-MAR-77 <233> [20,20]
ESMLDR.TSK             32.      12-MAR-77 <233> [20,20]
MDMPL.TSK              86.      12-MAR-77 <233> [20,20]

 TOTAL OF 697. BLOCKS IN 26. FILES

>
```

ESM TAPE #3 - MDMPL ASSEMBLER

```
FLX>CLO:=MT0:[20,20]*.*/LI

DIRECTORY       MT0:[20,20]
26-FEB-77

FASS.ODL                1.      26-FEB-77 <233>
MDMLST.CMD              1.      26-FEB-77 <233>
SUSAN.FOR               13.     26-FEB-77 <233>
BLOCK.FOR               3.      26-FEB-77 <233>
RESCAN.FOR              7.      26-FEB-77 <233>
WRT.FOR                 9.      26-FEB-77 <233>
SQUASH.FOR              3.      26-FEB-77 <233>
SCAN.FOR                5.      26-FEB-77 <233>
COLUMN.FOR              7.      26-FEB-77 <233>
CONDIT.FOR              11.     26-FEB-77 <233>
LITRL.FOR               13.     26-FEB-77 <233>
LOGIC.FOR               16.     26-FEB-77 <233>
LOGICA.FOR              13.     26-FEB-77 <233>
MDMPL.TSK               86.     26-FEB-77 <233>
SUSAN.OBJ               27.     26-FEB-77 <233>
BLOCK.OBJ               1.      26-FEB-77 <233>
RESCAN.OBJ              10.     26-FEB-77 <233>
WRT.OBJ                 11.     26-FEB-77 <233>
SQUASH.OBJ              3.      26-FEB-77 <233>
SCAN.OBJ                7.      26-FEB-77 <233>
COLUMN.OBJ              11.     26-FEB-77 <233>
CONDIT.OBJ              23.     26-FEB-77 <233>
LITRL.OBJ               23.     26-FEB-77 <233>
LOGIC.OBJ               38.     26-FEB-77 <233>
LOGICA.OBJ              38.     26-FEB-77 <233>

 TOTAL OF 380. BLOCKS IN 25. FILES

>
```

ESM TAPE #4 - DIAGNOSTICS

```
MCR>FLX TT1:=MT0:[*,*]*.*/LI

DIRECTORY       MT0:[0,0]
10-MAR-77

MEMCKO. OBJ              2.      26-FEB-77 <233> [1,4]
BLOUT. OBJ               2.      26-FEB-77 <233> [1,4]
LPCKO. OBJ               2.      26-FEB-77 <233> [1,4]
GTBO. OBJ                1.      26-FEB-77 <233> [1,4]
CRTOBJ. OBJ              2.      26-FEB-77 <233> [1,4]
PDPO. OBJ                1.      26-FEB-77 <233> [1,4]
GTBOA. OBJ               1.      26-FEB-77 <233> [1,4]
CTCGO. OBJ               2.      26-FEB-77 <233> [1,4]
PDP. OBJ                 6.      26-FEB-77 <233> [1,4]
CTCCO. OBJ               3.      26-FEB-77 <233> [1,4]
CONMEM. OBJ              5.      26-FEB-77 <233> [1,4]
BLKS. DAT                9.      26-FEB-77 <233> [1,4]
MEMCK. DAT               10.     26-FEB-77 <233> [1,4]
LPCK. DAT                8.      26-FEB-77 <233> [1,4]
PDP. DAT                 4.      26-FEB-77 <233> [1,4]
GTB. DAT                 4.      26-FEB-77 <233> [1,4]
GTBA. DAT                5.      26-FEB-77 <233> [1,4]
CTCG. DAT                11.     26-FEB-77 <233> [1,4]
CTCC. DAT                23.     26-FEB-77 <233> [1,4]
CRTCK. DAT               21.     26-FEB-77 <233> [1,4]
PDP. FOR                 3.      26-FEB-77 <233> [1,4]
PDP. TSK                 31.     26-FEB-77 <233> [1,4]
CONMEM. FOR              2.      26-FEB-77 <233> [1,4]
CONMEM. TSK              32.     26-FEB-77 <233> [1,4]
TI. DAT                  5.      10-MAR-77 <233> [1,4]
TI. OBJ                  1.      10-MAR-77 <233> [1,4]

 TOTAL OF 196. BLOCKS IN 26. FILES

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This publication is the User Manual for the Exploratory Systems Control Model (ESM). It describes the system, each capability and how to use it. This manual was prepared by Burroughs Corporation and is submitted in accordance with the requirements of contract DCA 100-75-C-0054.

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